LETTER

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High-frequency, scaled graphene transistors on diamond-like carbon

Yanqing Wu[1], Yu-ming Lin[1], Ageeth A. Bol[1], Keith A. Jenkins[1], Fengnian Xia[1], Damon B. Farmer[1], Yu Zhu[1] & Phaedon Avouris[1]

Owing to its high carrier mobility and saturation velocity, graphene has attracted enormous attention in recent years[1–5]. In particular, high-performance graphene transistors for radio-frequency (r.f.) applications are of great interest[6–13]. Synthesis of large-scale graphene sheets of high quality and at low cost has been demonstrated using chemical vapour deposition (CVD) methods[14]. However, very few studies have been performed on the scaling behaviour of transistors made from CVD graphene for r.f. applications, which hold great potential for commercialization. Here we report the systematic study of top-gated CVD-graphene r.f. transistors with gate lengths scaled down to 40 nm, the shortest gate length demonstrated on graphene r.f. devices. The CVD graphene was grown on copper film and transferred to a wafer of diamond-like carbon. Cut-off frequencies as high as 155 GHz have been obtained for the 40-nm transistors, and the cut-off frequency was found to scale as 1/(gate length). Furthermore, we studied graphene r.f. transistors at cryogenic temperatures. Unlike conventional semiconductor devices where low-temperature performance is hampered by carrier freeze-out effects, the r.f. performance of our graphene devices exhibits little temperature dependence down to 4.3 K, providing a much larger operation window than is available for conventional devices.

Graphene has zero bandgap, and therefore devices fabricated from it have a small on-off ratio. Although bandgap engineering techniques—such as nano-ribbon fabrication or the application of a strong displacement field to bilayer graphene—have been developed to open a small bandgap in graphene[15–19], the development of a reliable technique to create a sizable gap without degrading the electronic properties of the material remains challenging. On the other hand, a large on-off ratio is not necessary for many r.f. applications, such as amplifiers or mixers, and significant progress has been made in the development of high-performance r.f. transistors based on graphene materials produced by different synthesis techniques. For example, a maximum cut-off frequency of 300 GHz has been obtained for devices based on exfoliated graphene (ref. 11), and a maximum cut-off frequency of 100 GHz for devices based on epitaxial graphene grown on silicon carbide (ref. 9). In modern electronics, large volume production and low cost are crucial properties for any new technology. It has been shown that growing graphene on a Cu substrate by CVD can produce large-size, high-quality sheets at low cost[14]. Previous studies on r.f. transistors made from transferred graphene typically used silicon dioxide (SiO_2) as the substrate. However, graphene devices fabricated on SiO_2 have been found to suffer from additional scattering associated with the low surface phonon energy (59 meV) and large trap density in SiO_2, resulting in deterioration of both device properties and uniformity across the wafer. To mitigate these problems, here we introduce a new substrate for graphene r.f. transistors, namely, a diamond-like carbon (DLC) film grown on SiO_2. Compared to SiO_2 and most other substrates, the DLC film has a higher phonon energy (owing to the high phonon energy in diamond (165 meV)) and a lower surface trap density (DLC is non-polar and chemically inert)[20]. These desirable properties help the high performance of graphene r.f. transistors to be achieved.

Single-layer graphene was grown on copper foil at high temperatures close to 1,000 °C. Using a polymethylmethacrylate (PMMA) film as a protecting layer, the graphene sheet formed on Cu was then freed by dissolving the Cu using a solution of $FeCl_3$. The transfer process was completed by transferring the PMMA-graphene to the DLC substrate and subsequently removing the PMMA. Raman spectroscopy was used to verify the single-layer nature of the graphene after the transfer (see Supplementary Fig. 1). Arrays of graphene r.f. transistors on a DLC substrate were fabricated using a conventional top-down approach. The schematic view of the graphene r.f. transistor is shown in Fig. 1a. Electron-beam lithography was used to define the channel, source and drain contacts, and the gate electrodes. Oxygen plasma etching was used to remove graphene outside the channel. The source and drain contacts consist of a thin Pd film covered by a thicker Au film. The top-gate dielectric film includes an electron-beam-evaporated Al layer, which is then oxidized and an additional layer of Al_2O_3 grown by atomic layer deposition (ALD)[21]. We note that all fabrication process steps involve standard top-down approaches that can be readily implemented in high-throughput production. Figure 1b shows a scanning electron microscope (SEM) image of a dual-channel graphene r.f. transistor with a ground-signal-ground coplanar pad design suitable for r.f. measurements. Figure 1d shows an SEM image of the well-aligned fine structure of a device with a gate length of 40 nm. The transmission electron microscopy (TEM) image in Fig. 1c further confirms the excellent alignment between the gate and the source/drain electrodes and the gate length of 40 nm, the shortest demonstrated so far. This nearly perfect alignment with a small un-gated region of less than 20 nm in our transistors is critical for achieving good device performance. The access region between gate and source/drain is nearly constant for all the devices, regardless of their gate length.

Figure 1e shows the output characteristics of two graphene devices, one with a gate length of 550 nm (left) and one with a gate length of 40 nm (right). The drain voltage sweeps from 0 V to 1.6 V for the 550-nm device and from 0 to 1 V for the 40-nm device. The gate voltage changes from −8 V to 0 V, from bottom trace to top trace. As shown in the insets, the Dirac point voltage obtained from the long-channel (that is, long-gate) device is around −7 V as a result of impurity charge doping, possibly induced during the transfer process. We attribute this effect to fixed impurity doping rather than trap charges because of the very weak hysteresis and the temperature-independent position of the Dirac point observed in these devices. The gate modulation of the short-channel (that is, short-gate) device is much weaker than that of the long channel one. This is mainly due to the more dominant role of the contact resistance in short channel devices. Unlike the case of Si metal-oxide-semiconductor field-effect transistors (MOSFETs), there is currently no proven way to reduce the contact resistance of graphene transistors. Another cause of the weak modulation of the 40-nm device is the 'short-channel effect', in which the electrostatic control efficiency of the top gate is adversely affected by the drain voltage. Although this effect is well-studied for conventional Si MOSFETs, it is not well understood in graphene transistors, and may be even more severe in these devices owing to the conical graphene band structure and the occurrence of Klein tunnelling.

[1]IBM Thomas J. Watson Research Center, Yorktown Heights, New York 10598, USA.

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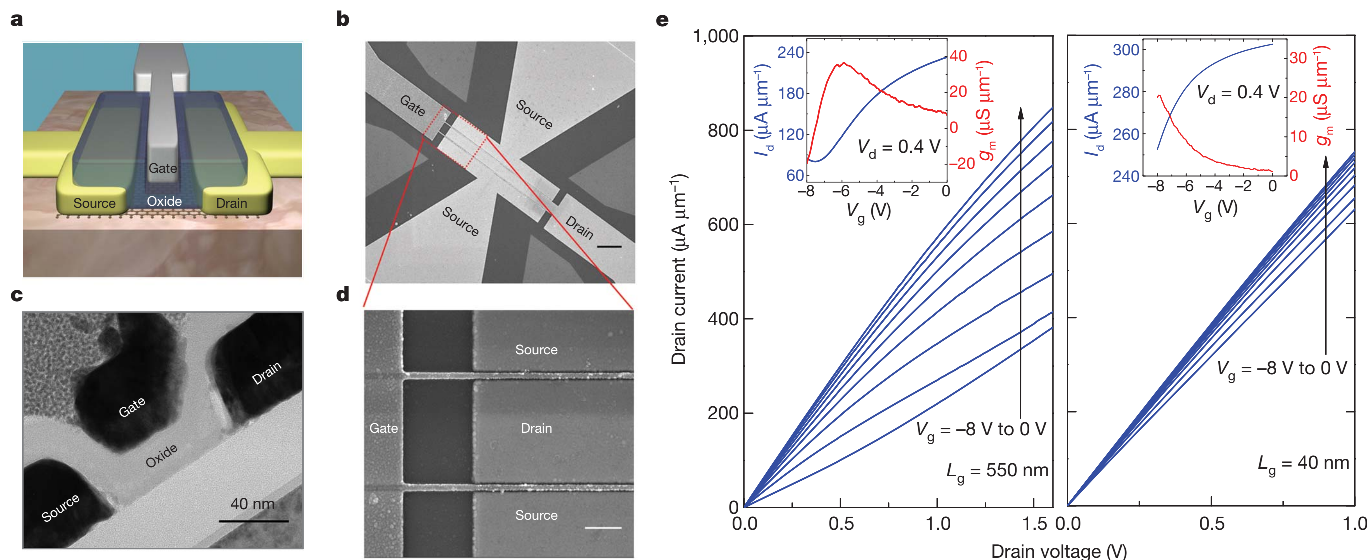

Figure 1 | Fabrication and output characteristics for graphene r.f. transistors. **a**, Schematic view of a top-gated graphene r.f. transistor on DLC substrate. **b**, SEM image of a typical top-gated dual-channel r.f. device. Scale bar, 3 μm. **c**, Cross-section TEM image of a graphene transistor with a gate length of 40 nm. Scale bar, 40 nm. **d**, SEM image of the 40-nm device. Scale bar, 400 nm. **e**, d.c. output characteristics of a 550-nm device (left) and a 40-nm device (right). Insets, transfer characteristics at drain–source voltage $V_{ds} = 0.4$ V.

High-frequency scattering parameters (S) of the graphene r.f. transistors were measured up to 30 GHz by an Agilent E8364C network analyser using standard ground-signal-ground probes (details of the measurement set-up and procedures are given in the Methods Summary). We used a de-embedding procedure that took account of parasitic effects (such as pad capacitance and wire resistance). This is achieved by measuring on-chip, inactive, 'open' and 'short' test devices; in the former, there was no graphene, and in the latter, gate, source and drain electrodes were all connected by metals. High fidelity in the de-embedding process was achieved by ensuring that the layouts of these open and short structures were strictly identical to that of the active device. The cut-off frequency (f_T), defined as the frequency at which the current gain becomes unity, is one of the most important figures-of-merit for evaluating the performance of r.f. devices. In Fig. 2a, the current gain, calculated from S parameters, is plotted against frequency f; a peak cut-off frequency f_T of 26 GHz is obtained for the 550-nm-long device at room temperature. To verify the value of f_T independently, Gummel's method[22,23] was adopted, and the same value of f_T was obtained, as shown in the inset of Fig. 2a. The current gain of devices with shorter gate lengths ($L_g = 140$ nm and 40 nm) is plotted in a similar fashion in Fig. 2b and c, respectively. A cut-off frequency of 70 GHz was obtained for the 140-nm transistor from both the intercept of the $1/f$ dependence and Gummel's method. An f_T as high as 155 GHz was obtained from the 40-nm-long device; this is the highest cut-off frequency yet achieved on CVD graphene, and 40 nm is also the smallest gate length reported so far. Although the direct current transconductance (g_m) suffers from the short-channel effect at this gate dimension, as discussed above, the overall r.f. performance benefits from the reduction of gate length.

In a well-behaved field-effect transistor (FET), the cut-off frequency can be related to g_m by the following equation[9]: $f_T = g_m/2\pi C_g$, where $C_g = \varepsilon_0\varepsilon_r W_g L_g/t_{ox}$. Here C_g is the gate capacitance, ε_0 is the dielectric constant of vacuum, ε_r is the relative dielectric constant of the gate dielectric, W_g is the channel width, L_g is the gate length and t_{ox} is the gate dielectric thickness. Therefore, the product $f_T L_g$ is expected to be linearly proportional to g_m for devices with the same gate dielectric and width, and the slope of a plot of f_T L_g versus g_m is determined only by the physical thickness of the gate oxide. Such a plot of $f_T L_g$ against g_m for three different gate lengths is shown in Fig. 3a; it exhibits the expected linear dependence, with a slope independent of the gate

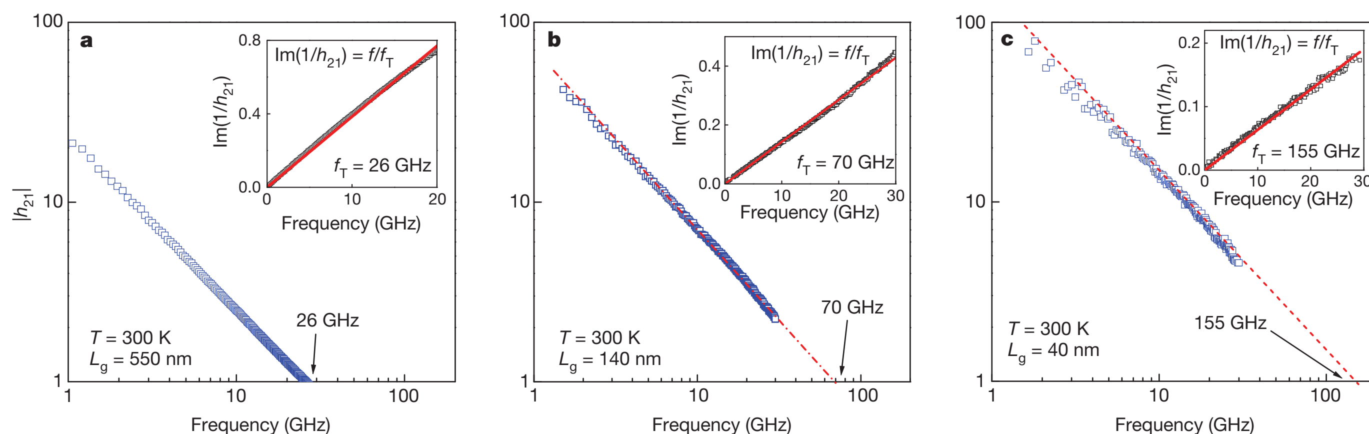

Figure 2 | Cut-off frequencies for three different devices at room temperature. Small-signal current gain $|h_{21}|$ versus frequency for devices with a gate length of 550 nm (**a**), 140 nm (**b**) and 40 nm (**c**) at room temperature. Intercepts give the cut-off frequency as 26 GHz, 70 GHz and 155 GHz, respectively. Insets, linear fitting using Gummel's method, showing extrapolated cut-off frequencies identical to the value obtained in the main panel for each device.

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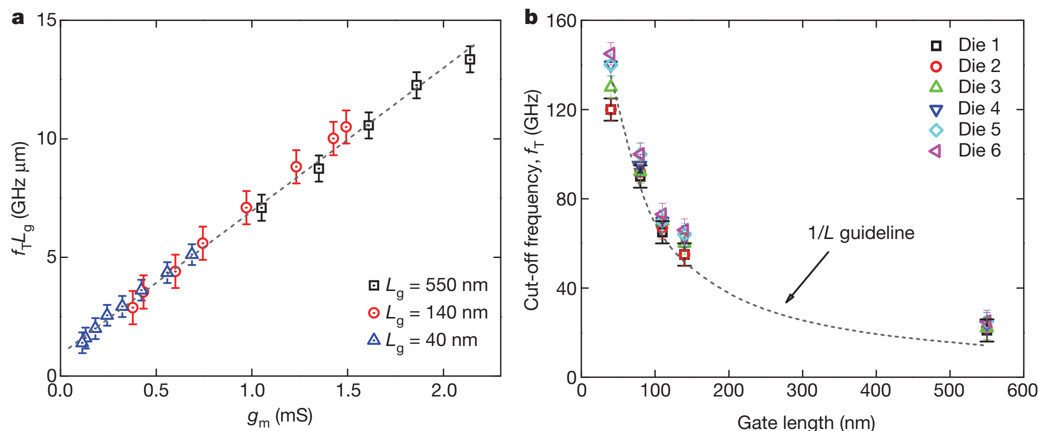

Figure 3 | Scaling behaviour of cut-off frequencies with gate length down to 40 nm. **a**, $f_T L_g$ versus direct current transconductance for three gate lengths: 550 nm (black squares), 140 nm (red circles) and 40 nm (blue triangles). The data from three different types of devices fall onto the same line, the slope of which corresponds to the unit area gate capacitance. This shows the uniformity of the graphene devices, the consistency of the measurements and the accuracy of the de-embedding approach. Data are shown as mean ± s.d., $n = 6$. **b**, Peak f_T as a function of gate length from 30 devices in 6 different dies located on the same wafer. Data are fitted well by the curve showing a $1/L_g$ dependence. Data are shown as mean ± s.d., $n = 3$.

lengths. This shows the uniformity of our devices across the whole wafer, and also demonstrates the measurement reliability. A high value of $f_T L_g = 13$ GHz μm is obtained for the 550-nm device; this is significantly higher than the value of 9 GHz μm for Si MOSFETs obtained from the International Technology Roadmap for Semiconductors (ITRS)[24], and is getting close to the best experimental results for Si MOSFETs.

To further test device uniformity and to examine device variation across the wafer, a systematic study of graphene transistors with five different gate lengths was performed; the results are shown in Fig. 3b. For each gate length, six devices from different dies (each die contains a complete set of devices) on the same wafer are measured and the peak cut-off frequencies are plotted. The performance variation is very small for all devices with the same gate length, as can be seen from Fig. 3a and b. Also, a $1/L_g$ dependence (the 'scaling trend') of the peak cut-off frequency is shown here, and is valid for devices with short gate lengths, even at the scaling limit of 40 nm. Previously, a $1/L_g^2$ dependence for f_T was observed for graphene FETs with long gate lengths where the transport is channel-resistance limited, partly owing to the severe mobility degradation associated with non-optimized gate dielectrics[8]. The $1/L_g$ scaling trend observed in our devices indicates that the transport is in a contact-limited regime, so that the electric field along the channel is dominated by the value of contact resistance at the source and drain and has little gate-length dependence. We note here that a similar $1/L_g$ dependence is usually observed for short-channel conventional Si and III–V FETs. This dependence is mainly due to the nearly-constant effective carrier velocity (obtained by reaching the saturation velocity of the material), which is seldom observed in current graphene devices. The long-channel (550-nm) device is in the region of transition from channel-limited transport to contact-limited transport. The f_T values obtained for this gate length are higher than the $1/L_g$ trend line; this is partly due to minimal short-channel effect for this relatively long gate.

In devices made from conventional semiconductors, the electrostatic potential profile will be controlled partly by the drain bias when the gate length is reduced. The resulting threshold voltage shift and drain-induced barrier lowering cause deterioration of the transistor switching. As in Si MOSFETs, controlling short-channel behaviour is of vital importance for graphene transistors. Moreover, occurrence of Klein tunnelling in graphene p–n junctions would make the short-channel effect worse[25–27]. Therefore, the transconductance is expected to decrease upon gate length scaling. The trade-off between performance and small device size will be the key factor in determining the scaling limit of graphene transistors. Nevertheless, as shown in Figs 2c, 3b and 4c, the 40-nm top-gated CVD graphene transistor on DLC is still well-behaved, with high r.f. performance. The result also shows the great potential for graphene transistors to be scaled even further, to a much smaller device size.

Many interesting studies of graphene physics, including investigations of the quantum Hall effect, have been performed at low temperatures: in contrast, no graphene r.f. transistors have been operated and studied below room temperature. A number of applications require cryogenic operation of r.f. devices, and how the graphene r.f. device performs at low temperatures is also scientifically important. Here we carried out the first study of graphene r.f. transistors down to liquid helium temperatures. Care was taken to ensure measurement accuracy; this included calibrating the system after the probe temperature and sample temperature had reached equilibrium. We found that—unlike many previous studies of graphene on SiO_2 substrates which showed strong temperature-dependent interface trap density and occupation—the r.f. performance of the graphene devices on DLC showed very little, if any, temperature dependence, being essentially unchanged at 4.3 K (Fig. 4a and b). Different gate biases were applied (from −8 V to 0 V) with a fixed drain bias of 1.6 V in a 550-nm-long device, where the current gain follows a $1/f$ dependence between 300 K and 4.3 K. This stability with temperature illustrates a significant advantage of the high quality DLC substrate, in which the trap density is very low. Figure 4c shows the current gain as a function of frequency for three devices with different gate lengths at 4.3 K; all exhibit a well-defined $1/f$ dependence, as at room temperature. As shown in the summary plot in Fig. 4d, the cut-off frequency shows little temperature dependence in the range from 300 K to 4.3 K. Unlike the carrier freeze-out effects typically observed in Si MOSFETs at cryogenic temperatures[28], the consistent temperature-independent results found here open up new opportunities for future graphene r.f. applications, such as ultra-low-noise or outer-space operations.

Besides the cut-off frequency, another important figure of merit for r.f. devices is the available power gain[28,29]; this is assessed using the maximum oscillation frequency (f_{MAX}), defined as the frequency at which the power gain is equal to one. Very low power gain has been achieved previously with graphene r.f. devices, and it was therefore seldom reported. The poor f_{MAX} of graphene devices usually results from the lack of clear current saturation and non-optimized gate structure. Here we show that despite the lack of clear saturation, we can achieve a high f_{MAX} of 20 GHz from the 550-nm device and 13 GHz from the 140-nm device (see Supplementary Fig. 4). It is noted that f_{MAX}, unlike f_T, is highly dependent on the design of the device and on the details of the interconnects, such as the gate metal thickness.

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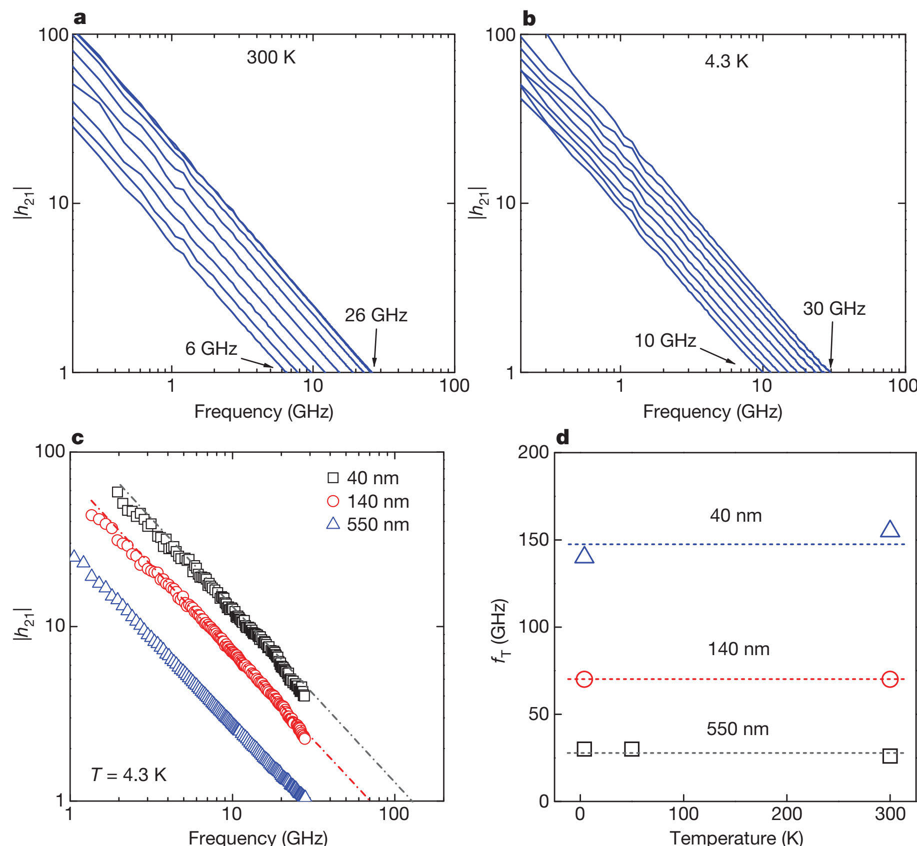

Figure 4 | Temperature dependence of cut-off frequency for different devices. **a**, **b**, Current gain as a function of frequency at 300 K (**a**) and 4.3 K (**b**). The gate length is 550 nm, with a V_{ds} of 1.6 V and with V_{gs} varying from −8 V to 0 V. **c**, Current gain versus frequency for three values of L_g (550 nm, 140 nm and 40 nm) at 4.3 K. The value of f_T is 28 GHz, 70 GHz and 140 GHz, respectively. **d**, Summary plot of the temperature dependence of f_T for three different devices; little temperature dependence was found.

Use of an optimized design, such as a mushroom-shaped gate to reduce the gate resistance, is expected to further improve f_{MAX}.

The r.f. performance of graphene is limited mainly by two factors: the substrate-limited carrier mobility and the contact resistance. Whereas the mobility dominates in long-channel devices, contact resistance becomes more critical as the gate length decreases. To further improve the r.f. performance of the graphene devices, efforts should be made to minimize the contact resistance, as short-channel devices are best suited to achieving ultimate device performance and high-density circuits. The contact resistance of graphene transistors is currently typically up to an order of magnitude higher than that of Si MOSFETs. Also, the short-channel effect can be mitigated by scaling down the thickness of the gate dielectric to achieve better electrostatic control by the gate.

METHODS SUMMARY

Top-gated graphene r.f. transistors were fabricated using graphene grown by CVD on copper[14], as follows. After evacuation of the CVD chamber, the Cu foil was heated to 875 °C in forming gas (H_2/Ar) and kept at this temperature for 30 min. After reduction, the Cu foil was exposed to ethylene at 975 °C for 10 min and then cooled. PMMA was spin-coated on top of the graphene layer that had formed on one side of the Cu foil. The Cu foil was then dissolved in 1 M iron chloride solution. The remaining graphene/PMMA layer was washed and transferred to the desired substrate. Subsequently, the PMMA was dissolved by treatment with hot acetone for one hour. The CVD graphene after transfer to DLC was characterized by Raman spectroscopy before device fabrication. DLC film was grown on an 8-inch Si substrate using cyclohexane (C_6H_{12}) with a vapour pressure of 1.8 p.s.i. in a CVD chamber. The flow rate was typically 25–40 cm^3 STP per min at 100 mtorr pressure. The DLC growth rate is 32 Å s^{-1} at 60 °C; this was followed by an anneal step at 400 °C for 4 h. The source/drain contact was 20 nm Pd/30 nm Au deposited by electron-beam evaporation. The gate oxide was formed by an oxidized Al layer deposited by electron-beam evaporation, followed by the deposition of 15 nm ALD Al_2O_3 film. The direct current and r.f. characterizations were carried out in a probe station under $<10^{-6}$ torr using an Agilent parameter analyser B1500, and a E8364C network analyser. The system was calibrated using a short-open-load-through method. On-chip open and short structures with the exact design of the devices were used to de-embed parasitic effects, such as pad capacitance and interconnection resistance. The low-temperature measurements were performed using the same approach, and system calibration was done for each temperature. On-chip de-embedding, using standard open-short structures, was also done at each temperature.

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Supplementary Information is linked to the online version of the paper at www.nature.com/nature.

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