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Ambipolar-to-Unipolar Conversion of Carbon Nanotube Transistors by Gate Structure Engineering

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ABSTRACT

The switching behavior of carbon nanotube field-effect transistors (CNFETs) can be improved by decreasing the gate oxide thickness. However, decreasing the oxide thickness also results in more pronounced ambipolar transistor characteristics and higher off-currents. To achieve high-performance unipolar CNFETs as required for CMOS logic gates, we have fabricated partially gated CNFETs with an asymmetric gate structure with respect to the source and drain electrodes. With our gate structure engineering concept, *p*-type CNFETs have been fabricated from an ambipolar CNFET. It is also found that fringing fields from source and drain are important in determining the CNFET behavior as the device size decreases.

Carbon nanotubes (CNs) have attracted much attention because of their unique physical and electrical properties resulting primarily from their one-dimensional structure.[1] Carbon nanotube field-effect transistors (CNFETs) with characteristics comparable to or exceeding state-of-the-art Si-based transistors have been demonstrated using a conventional FET design,[2,3] showing that CNFETs are promising candidates for high-performance nanoscale electronic applications.

From the application's point of view, both *n*- and *p*-type FETs that operate in the same voltage range are necessary to achieve CMOS-like logic gates, the basic units of computers. Early studies showed that, without intentional doping, most CNFETs operate as *p*-type FETs in air, and they can be transformed into ambipolar or *n*-type devices in vacuum.[4] Basic logic gates based on CNFETs have been recently demonstrated by several groups.[3,5,6] More recently, efforts have been made to improve the switching behavior of CNFETs by decreasing the gate oxide thickness t_{ox}[2,6] and/or by adopting high-κ dielectric materials.[7,8] However, CNFETs possess very different scaling behavior from conventional transistors[9,10] because of the Schottky barrier (SB) contacts formed at the nanotube/metal interface.[7,11,12] As a result, vertically scaled CNFETs exhibit more pronounced ambipolar characteristics,[10] rather than the *p*-type behavior usually observed in devices fabricated with a thick gate oxide.[13]

CNFETs studied here are fabricated using the standard back-gate geometry.[14] Single-wall carbon nanotubes with an average diameter d_t of 1.4 nm[15] are dispersed on a *p*-type Si substrate covered by a thin layer (10 nm) of thermally grown SiO_2. The Si substrate serves as the back gate, and source and drain contacts are made of 50-nm-thick titanium (Ti). Figures 1a and b show the drain current I_d as a function of gate voltage V_{gs} for two typical CNFET devices at different drain voltages (V_{ds}) measured in air. Two sets of CNFET characteristics are explicitly shown here to illustrate the device-to-device variations in these CNFETs. In particular, the tube diameter variation in these CNFETs may result in an off-current I_{off} (the minimum I_d as a function of V_{gs}) that differs by orders of magnitude between different devices, as shown in Figures 1a and b. For the sake of discussion, we denote CNFETs that exhibit low off-currents ($I_{off} \leq 0.1$ nA) at $V_{ds} = -0.7$ V as type-A CNFETs (e.g., Figure 1a) and those with $I_{off} > 0.1$ nA as type-B devices (e.g., Figure 1b). We note that type-B devices usually also possess higher on-currents I_{on} and a stronger V_{ds} dependence than type-A CNFETs (see Figures 1a and b). All of these observations are consistent with the notion that type-B devices are likely to be CNFETs involving nanotubes with larger d_t.

Despite the distinct I_{off} for type-A and B CNFETs, both devices exhibit clear ambipolar characteristics because of the thin gate oxide used here, as shown in Figures 1a and b. Figures 1c and d depict schematic band diagrams for CNFETs at different V_{gs}, showing that one branch (*p*-type) of I_d results from hole injection from the source (see Figure 1c), while the other branch (*n*-type) is due to the electron injection from the drain (see Figure 1d). The use of a thin gate oxide also results in a rapid increase in the off-current with drain voltage.[10] As shown in Figure 1b, the off-current

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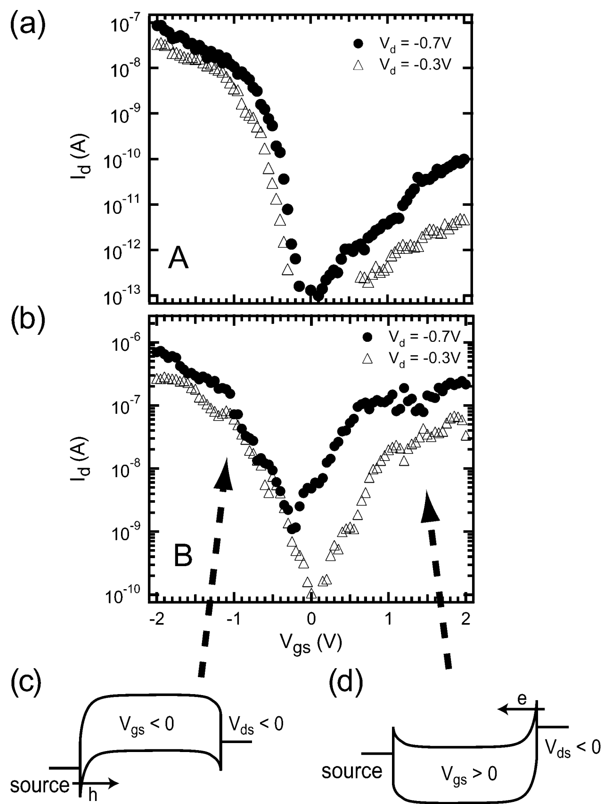

Figure 1. Panels (a) and (b) plot I_d vs V_{gs} of two typical CNFETs measured in air at different V_{ds}. The drain/source distance is 300 nm and the bottom gate oxide is SiO_2 with a thickness of 10 nm. The CNFET in (a) exhibits an off-current ≤ 0.1 nA at $V_{ds} = -0.7$ V and is denoted as a type-A device. The device in (b) possesses a higher off-current and is categorized as type B. Schematic band diagrams of nanotubes at different V_{gs} are shown in (c) and (d) to explain their ambipolar characteristics.

I_{off} is ~80 pA at $V_{ds} = -0.3$ V and increases to 1 nA at $V_{ds} = -0.7$ V. The higher I_{off} implies a higher power dissipation in the OFF state as well as a lower on/off current ratio for the transistor. We note that both the ambipolar behavior and higher I_{off} are undesirable for CMOS-like logic gate designs, since they prevent vertical scaling to small oxide thicknesses in CNFETs and severely limit the allowed range of drain voltages for high-performance transistor functions.

In order to take advantage of the improved on-state characteristics of thin-oxide CNFETs in CMOS circuit designs, it is essential to suppress one of the branches in the ambipolar subthreshold characteristics as shown in Figure 1a or b. In this paper, we transform thin-oxide CNFETs that possess ambipolar characteristics into unipolar transistors by introducing an asymmetry between the source and drain electrostatics as proposed in ref 16. The asymmetry is obtained by creating a deep trench underneath the nanotube near one of the source/drain contacts. In that way, only part of the carbon nanotube is electrostatically controlled through the back gate. The results of the partially gated CNFETs not only show proof-of-principle of gate structure engineering to improve the CNFET performance but also point out a novel approach to fabricate *p*- or *n*-type CNFETs that are stable in ambient environments. It is also found that the current suppression in one branch depends on the trench width, and that as the trench width decreases, the CNFET behavior is increasingly affected by fringing fields due to the source/drain electrodes. This fringing field effect becomes more important when scaling the device to smaller sizes and should be taken into account for device optimization.

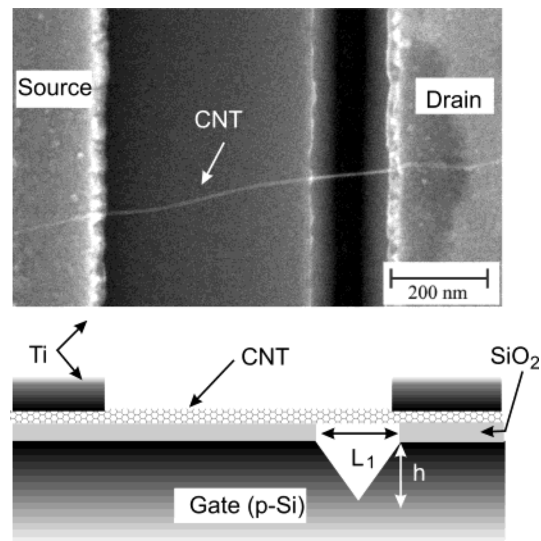

Figure 2. (Top) SEM image of a partially gated CNFET. The source/drain separation is $L = 590$ nm and the trench width is $L_1 = 160$ nm. (Bottom) Schematic of the device cross section, showing a V-shaped groove in Si.

To fabricate partially gated CNFETs, poly(methyl methacrylate) (PMMA) is spin-coated onto as-prepared devices, and a narrow window is created between two Ti contacts by electron beam (EB) lithography. The gate oxide and Si substrate exposed by the PMMA window are then wet-etched by NH_3-buffered HF and potassium hydroxide (KOH) solutions, respectively.[17] The etch window is designed to be positioned close to and partly overlapping with one of the Ti contacts to ensure an asymmetric gate geometry at the two nanotube/metal interfaces. Figure 2 shows the SEM image of a partially gated CNFET that has a trench of width $L_1 \sim 160$ nm located near the right Ti contact. Due to the anisotropic etch rate of Si in KOH solutions,[17] a V-shaped groove with a height of $h \sim 60$ nm is formed in the Si substrate, as shown by the schematic device cross section in the bottom of Figure 2. SEM images of these partially gated CNFETs are also taken at a slant angle, indicating that the nanotubes are suspended across the trench without touching the bottom gate.

Figure 3a shows subthreshold characteristics $I_d(V_{gs})$ of a partially gated CNFET for $V_{ds} = -0.3$ and -0.7 V with a 160-nm wide trench, exhibiting clear *p*-type unipolar characteristics. The source electrode is chosen as the left contact and grounded, while the drain refers to the right contact close to the trench (see Figure 2). This partially gated CNFET is fabricated from a type-A device, and the subthreshold characteristics of the original CNFET prior to trench etching are shown in Figure 1a. The *p*-type branch in Figure 3a shows an on/off current ratio > 10^4 at $V_{ds} = -0.7$ V and a subthreshold slope, defined as $S = (\mathrm{d}\log I_d/\mathrm{d}V_{gs})^{-1}$, of $S \sim 130$ mV/decade, comparable to the S value of 120 mV/decade

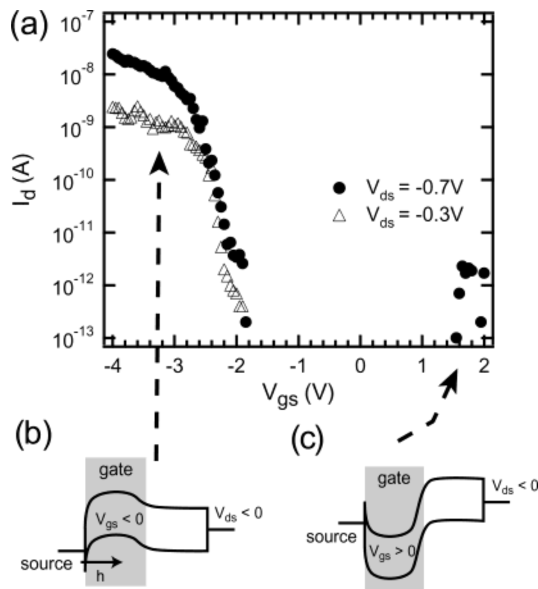

Figure 3. (a) Subthreshold characteristics $I_d(V_{gs})$ of the partially gated CNFET shown in Figure 2. The CNFET was a type-A device with subthreshold characteristics shown in Figure 1a before trench etching. The drain electrode is chosen as the right contact located close to the trench, while the source is chosen as the left contact. The band diagrams of the partially gated CNFET are depicted for (b) $V_{gs} < 0$ (*p*-branch) and (c) $V_{gs} > 0$ (*n*-branch).

of the original device before trench etching. We note that while the *p*-type branch in Figure 3a resembles that of a fully gated CNFET, the *n*-type current is substantially suppressed[18] and there is no drain-induced barrier lowering (DIBL)-like behavior in the partially gated CNFET. The small currents (~pA) at high positive gate voltages ($V_{gs} \geq 1.5$ V) for $V_{ds} = -0.7$ V are within the noise level. Note that the gate voltage sweeping range has been extended to −4 V for the measurement in Figure 3a. In comparison with Figure 1a, measuring at more negative V_{gs} results in a threshold voltage[19] shift of ~ −1.5 V.[20]

Figures 3b and c depict qualitative band diagrams of the partially gated CNFET for $V_{gs} < 0$ (*p*-type) and $V_{gs} > 0$ (*n*-type), respectively. As a first approximation, the band diagrams assume that the bottom gate has no influence on the nanotube in the trench region (the ungated segment); limitations of this approximation are discussed later. In Figures 3b and c, we note that the band bending near the source electrode is similar to that in the case of a fully gated CNFET (see Figures 1c and d), regardless of the trench at the drain. Therefore, for $V_{gs} < 0$, the gate field reduces the SB thickness at the source to enable hole tunneling, and the CNFET is turned on. However, the on-current of partially gated CNFETs may be lower than that of their fully gated counterparts, especially at small drain biases, because of a potential barrier at the gated/ungated interface for partially gated CNFET (see Figure 3b) that contributes to increased backscattering in the nanotube channel. As shown in Figure 3a, the partially gated CNFET exhibits a more pronounced I_{on} reduction as $|V_{ds}|$ decreases than in the case of the original CNFET shown in Figure 1a. On the other hand, for the partially gated CNFET at $V_{gs} > 0$, most of the band bending occurs across the gated/ungated interface region, and there is little band bending at the drain contact (see Figure 3c). The thick Schottky barrier at the drain prevents electron injection into the nanotube, resulting in a significantly lower *n*-type branch current, and thus the CNFET remains off for $V_{gs} > 0$. The results here demonstrate gate structure engineering to improve and manipulate the CNFET characteristics.

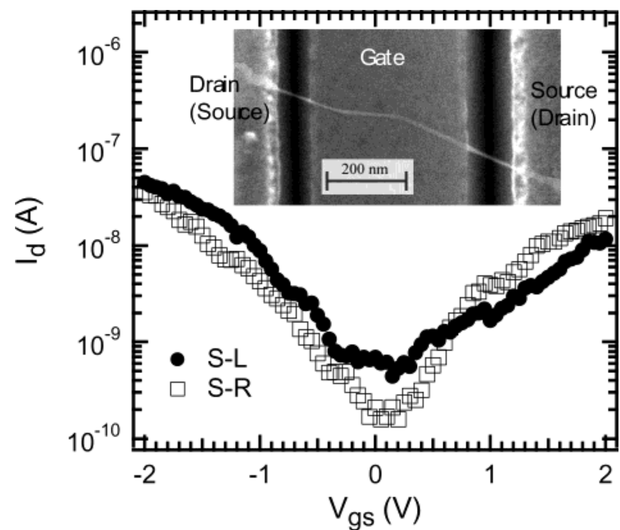

Figure 4. Subthreshold characteristics of a CNFET having two trenches of widths of 85 and 110 nm at the left and right contacts, respectively. The CNFET was a type-B device before trench etching. Measured $I_d(V_{gs})$ at $V_{ds} = -0.3$ V are represented by (●) when the left contact is chosen to be the source and (□) for right contact to be the source. The inset shows the SEM image of this CNFET device.

We have also fabricated partially gated CNFETs with different trench widths L_1 to study the effect of fringing fields. We find that in order to obtain a good unipolar behavior, as shown in Figure 3a, a sufficiently large L_1 is required to effectively suppress the carrier injection from the contacts. Figure 4 shows the transfer characteristics of a partially gated CNFET ($V_{gs} = -0.3$ V) with two trenches of smaller widths ~85 and 110 nm at both contacts, as shown by the inset of Figure 4. This double-trenched CNFET is fabricated from a type-B device before trench etching, so that the current is above the noise level even for the off-state to facilitate the observation of fringing field effects. In Figure 4, two source/drain configurations are denoted as S−L and S−R to represent the source at the left contact (●) and at the right (□), respectively. It is noted that, with trenches at both drain and source electrodes, the CNFET exhibits ambipolar characteristics and can still be switched on and off by the bottom gate with an on/off current ratio ≥ 30. The reason that the device is *not* always off in the presence of trenches at both contacts is due to the fringing field effects that become more important as the trench width decreases. These additional field impacts, not considered in our simple band diagrams, consist of gate fields emerging from the V-shaped groove and/or the fringing fields from the metal (Ti) contacts. These fringing fields can weakly modulate the SB thickness, control carrier injection from the contacts, and result in larger S values than for the fully gated CNFETs, similar to the case of a thick oxide.[7] As shown in Figure 4,

$S \sim 580$ and 660 mV/decade for the p-type branch in the S−L and S−R configurations, respectively. CNFETs showing unexpected characteristics due to fringing fields from nearby electrodes have been reported in the past[3,22] and predicted by simulations.[23] Fringing fields become more important when the channel length of a CNFET is reduced, and they should be taken into account in device optimization. The combined results of Figures 3a and 4 indicate that for the oxide and Ti thickness used here, a trench width $\gtrsim 160$ nm is sufficient to avoid the fringing field impacts.

It has been suggested that nanotubes show p-type doping behavior on a SiO_2 substrate but are intrinsic when suspended.[24] Our results, however, are not consistent with this notion. If indeed our tubes would exhibit a different "doping profile" after the trench formation than before, one would expect a shift in the threshold voltage. On the contrary, as shown by Figures 1b and 4, the CNFET with trenches exhibits a similar threshold voltage as the fully gated CNFET, indicating that the effects of doping variation between gated and suspended nanotube sections, if any, are negligible in our experiments.

In conclusion, we have transformed an ambipolar CNFET into a unipolar p-type CNFET by a partial gate structure where a deep trench is created near the drain contact. The results demonstrate proof-of-principle of gate structure engineering to improve and manipulate the performance of CNFETs for desired applications, e.g., to obtain unipolar CNFETs for CMOS-like logic gates. We note that n-type CNFETs may also be obtained by eliminating the p-type branch of an ambipolar CNFETs with a similar partial gate structure. It is found that due to the fringing field effects, a sufficiently large trench width is required to achieve satisfactory unipolar characteristics.

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References

(1) Dresselhaus, M. S.; Dresselhaus, G.; Avouris, Ph. *Carbon nanotubes: synthesis, structure, properties, and applications*; Springer-Verlag: Berlin, 2001.
(2) Wind, S. J.; Appenzeller, J.; Martel, R.; Derycke, V.; Avouris, Ph. *Appl. Phys. Lett.* **2002**, *80*, 3817.
(3) Javey, A.; Kim, H.; Brink, M.; Wang, Q.; Ural, A.; Guo, J.; McIntyre, P.; Lundstrom, M.; Dai, H. *Nature Mater.* **2002**, *1*, 241.
(4) Derycke, V.; Martel, R.; Appenzeller, J.; Avouris, Ph. *Appl. Phys. Lett.* **2002**, *80*, 2773.
(5) Derycke, V.; Martel, R.; Appenzeller, J.; Avouris, Ph. *Nano Lett.* **2001**, *1*, 453.
(6) Bachtold, A.; Hadley, P.; Nakanishi, T.; Dekker, C. *Science* **2001**, *294*, 1317.
(7) Appenzeller, J.; Knoch, J.; Derycke, V.; Martel, R.; Wind, S. J.; Avouris, Ph. *Phys. Rev. Lett.* **2002**, *89*, 126801.
(8) Javey, A.; Wang, Q.; Ural, A.; Li, Y.; Dai, H. *Nano Lett.* **2002**, *2*, 929.
(9) Appenzeller, J.; Knoch, J.; Martel, R.; Derycke, V.; Wind, S. J.; Avouris, Ph. *IEDM Digest* **2002**, 285.
(10) Radosavljevic, M.; Heinze, S.; Tersoff, J.; Avouris, Ph. *Appl. Phys. Lett.* **2003**, *83*, 2435.
(11) Freitag, M.; Radosavljevic, M.; Zhou, Y. X.; Johnson, A. T.; Smith, W. F. *Appl. Phys. Lett.* **2001**, *79*, 3326.
(12) Heinze, S.; Tersoff, J.; Martel, R.; Derycke, V.; Appenzeller, J.; Avouris, Ph. *Phys. Rev. Lett.* **2002**, *89*, 10681.
(13) Avouris, Ph.; Appenzeller, J.; Martel, R.; Wind, S. J. *Proc. IEEE* **2003**, *91*, 1772.
(14) Martel, R.; Schmidt, T.; Shea, H. R.; Hertel, T.; Avouris, Ph. *Appl. Phys. Lett.* **1998**, *73*, 2447.
(15) Thess, A.; Lee, R.; Nikolaev, P.; Dai, H.; Petit, P.; Robert, J.; Xu, C.; Lee, Y. H.; Kim, S. G.; Rinzier, A. G.; Colbert, D. T.; Scuseria, G. E.; Tomanek, D.; Fischer, J. E.; Smalley, R. E. *Science* **1996**, *273*, 483.
(16) Heinze, S.; Tersoff, J.; Avouris, Ph. *Appl. Phys. Lett.* **2003**, *83*, 5038.
(17) Seidel, H.; Csepregi, L.; Heuberger, A.; Baumgartel, H. *J. Electrochem. Soc.* **1990**, *137*, 3612.
(18) We use the terms "substantial suppression", "eliminate", and "significant lowering" to indicate a current reduction of at least 2 orders of magnitude.
(19) The threshold voltage is defined as the gate voltage at which the current I_d deviates from the exponential dependence in the subthreshold region.
(20) As we have verified by changing the V_{gs} range back to the former condition used in Figure 1a, this shift can be reversed, implying that it results from charge traps in the oxide[21] rather than a doping effect.
(21) Radosavljevic, M.; Freitag, M.; Thadani, K. V.; Johnson, A. T. *Nano Lett.* **2002**, *2*, 761.
(22) Wind, S. J.; Appenzeller, J.; Avouris, Ph. *Phys. Rev. Lett.* **2003**, *91*, 058301.
(23) Guo, J.; Wang, J.; Polizzi, E.; Datta, S.; Lundstrom, M. *IEEE Trans. Nanotech.* **2003**, *2*, 329.
(24) Minot, E. D.; Yaish, Y.; Sazonova, V.; McEuen, P. L. cond-mat/0402425 2004.

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