Comparing Carbon Nanotube Transistors - The ideal choice: A novel Tunneling Device Design

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***Abstract*— Three different carbon nanotube field-effect transistor (CNFET) designs are compared by simulation and experiment. While a C-CNFET with a doping profile similar to a "conventional" p- or n-MOSFET in principle exhibits superior device characteristics when compared with a Schottky barrier (SB-)CNFET, we find that aggressively scaled C-CNFET devices suffer from "charge pile-up" in the channel. This effect which is also known to occur in floating body silicon transistors deteriorates the C-CNFET off-state substantially and ultimately limits the achievable on/off-current ratio. In order to overcome this obstacle we explore the possibility of using carbon nanotubes as gate-controlled tunneling devices (T-CNFETs). The T-CNFET benefits from a steep inverse subthreshold slope and a well controlled off-state while at the same time delivering high performance on-state characteristics. According to our simulation, the T-CNFET is the ideal transistor design for an ultra-thin body three-terminal device like the CNFET.**

***Index Terms*— carbon nanotube, field-effect transistor, tunneling device**

I. Introduction

THE most promising nano-material to be used in future generations of nano field-effect transistors (nano-FETs) has been suggested to be the carbon nanotube (CN) [1]. While several major technology related questions still need to be addressed, it becomes increasingly obvious that from a material prospective and from the standpoint of electrostatics a semiconducting carbon nanotube is an excellent choice for a three-terminal FET design. In particular the possibility to obtain ballistic transport over several hundred nanometers at room-temperature [2], [3], [4] together with a very large Fermi velocity of around 10^8cm/s [5] allows for high performance on-state characteristics [6], [7], [8], [9]. At the same time, the large energetic spacing between one-dimensional (1D) subbands due to quantization along the tube perimeter results in energy gaps for semiconducting carbon nanotubes ranging from several hundred meV to more than 1eV depending on the tube diameter t_{ch} [5]. The right choice of t_{ch} can thus ensure in principle a good transistor off-state as well. The tube diameter also has direct relevance for the electrostatic control in a CNFET. Carbon nanotube FETs are ultra-thin body devices [10] that do not suffer from severe mobility degradation as typically observed for silicon MOSFETs with nanometer dimensions [11]. This makes nanotubes extremely suitable for aggressive scaling of the channel length well into the nanometer range while preserving long-channel type electrical characteristics [12].

With the intrinsic advantages of carbon nanotubes established, the main question to address is: "What device geometry is ideally suited to enable optimum device performance?" or "How do we make best use of the intrinsic potential of carbon nanotubes as three-terminal devices?" . In this article we will discuss the major benefits and disadvantages of various CN-based transistor designs using experimental results and simulations we have performed. We demonstrate through experiments and simulation that a novel device approach - the tunneling-CNFET (T-CNFET) is ideally suited for nanotube-based transistor applications in terms of both, intrinsic switching speed as well as power delay product.

Figure 1 illustrates the three different device concepts under consideration schematically. CN (i) denotes an undoped, intrinsic nanotube or portion of the same while CN (p) and (n) indicate doping of a certain segment of the nanotube. Different from case a), in cases b) and c) only part of the nanotube is gated. It is worth mentioning that our arguments apply whether the gate is located underneath or on top of the nanotube. In fact, tighter gate control can be achieved in all cases by wrapping the gate dielectric (called oxide in the figure) and the gate (typically a metal of appropriate work function) around the nanotube.

II. Electrical characteristics of SB-CNFETs and C-CNFETs and the disadvantages of the two designs

The two device concepts that have been discussed so far in the literature are the Schottky barrier (SB-)CNFET where metal source/drain contacts are directly connected to the gate controlled nanotube channel and the C-CNFET with a doping profile along the nanotube that resembles a "conventional" MOSFET. In fact, sophisticated doping profiles have only very recently been introduced into the design of nanotube devices [13], [14], [15]. There is a twofold reason that SB-CNFETs are still the most common CN device layout: First, controlled doping is not an easy task to accomplish since ion implantation techniques that are employed to create a doping profile in

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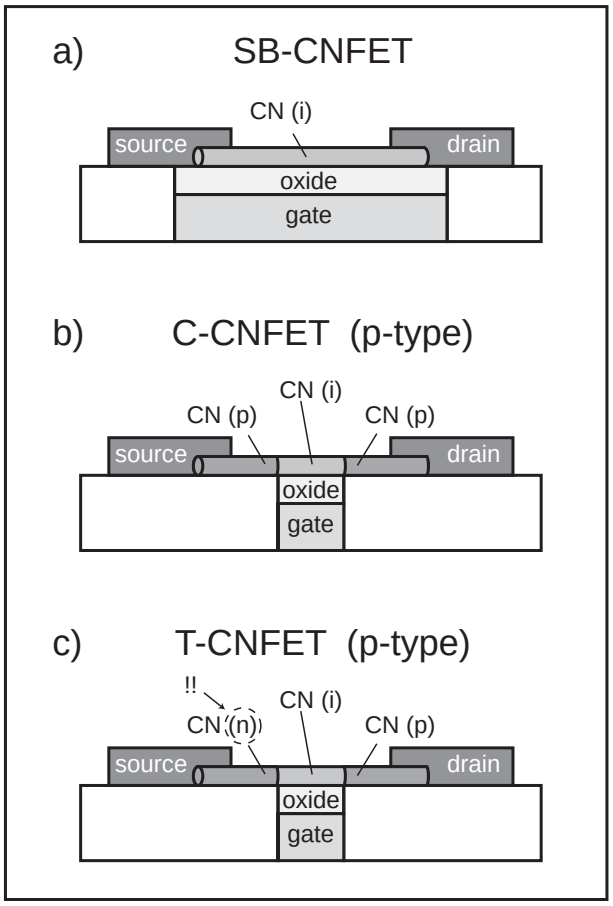

Fig. 1. The three device concepts under consideration. In case a) gating occurs over the entire nanotube channel including the contact areas. In b) and c) a p/i/p or n/i/p doping profile exists along the tube. Only the intrinsic portion of the nanotube is gated.

conventional semiconductors cannot be used in the case of nanotubes. The reason being that removing any carbon atoms that actually form the tube and replacing them by a dopant would destroy the desired nanotube properties. Thus doping of CNs requires controlling the electrostatics of the nanotube environment by molecules [13], additional gates [14] or metal ions [15] instead. Second, only if SB-CNFETs are aggressively vertically scaled by reducing the gate oxide thickness t_{ox} or by introducing high-k dielectrics some inherent disadvantages become apparent. Figure 2 illustrates this second fact for an SB-CNFET with a thin gate dielectric of $t_{ox} = 10$nm (SiO_2). Since the gate acts on the entire intrinsic nanotube channel up to the metal contacts, on-currents are observed for both negative and positive gate voltages. Ambipolar characteristics are obtained due to hole injection for negative gate voltages V_{gs} and electron injection for positive V_{gs} with a very distinct drain voltage (V_{ds}) dependence [12], [16], [17]. The insets of Fig. 2 show the current injection at the source and drain electrodes schematically. One key ingredient is that the width of the Schottky barrier at the metal/nanotube interface decreases with decreasing t_{ch} and t_{ox} [10], [18] such that electrons as well as holes can tunnel directly from the metal contact into the nanotube channel. In this sense, a carbon nanotube with a $t_{ch} \sim 1$nm always exhibits a rather small Schottky barrier width. The other important aspect is that transport inside the nanotube is ballistic and the drain voltage drops correspondingly exclusively at the electrodes.

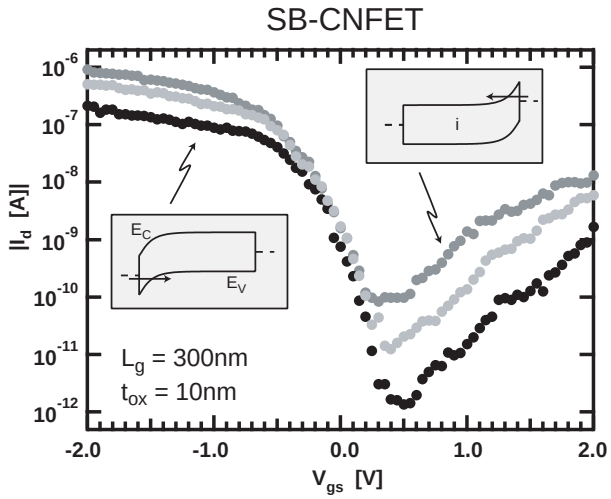

Fig. 2. Experimental data on a titanium contacted SB-CNFET for three different V_{ds} of -1.0V, -0.7V, and -0.4V.

Since switching always involves a change of the Schottky barrier width, the term Schottky barrier CNFET has been established to describe this type of nanotube device [19], [20]. The gate voltage alters the tunneling probability and thus the current through the device. This is true even for zero Schottky barrier height. While a clear advantage of a small Schottky barrier width is the ability to obtain decent on-currents in an SB-CNFET even for moderate barrier heights, it is also the ease of current injection that limits the achievable off-currents (I_{off}) as apparent from Fig. 2. The smaller the energy gap E_g of the nanotube used, the higher I_{off}. In addition, it has been pointed out that for an SB-CNFET the inverse subthreshold slope $S = dV_{gs}/d\log_{10} I_d$ is always larger than $\approx 60\mathrm{mV/dec}$ [20]. It is this set of arguments that makes it desirable to explore alternative device concepts.

Recently, it has been proposed to adopt a different scheme for a carbon nanotube based transistor. By introducing a p/i/p or n/i/n doping profile along the nanotube channel with highly doped areas close to the contacts and by gating only the undoped portion of the tube, so-called C-CNFETs (see figure 1b) have been realized [13], [14], [15]. These structures resemble conventional p- and n-type MOSFETs with the difference that the gated region is undoped as appropriate for an ultra-thin body device. The advantages of this approach are as follows: a) Due to the doping profile carrier injection of the minority carrier type (e.g. holes in an n-type C-CNFET) from the drain side is suppressed and unipolar device characteristics with low off-currents can be obtained. b) Since switching does

not involve the contact area close to the metal electrodes, I_{off} is limited by thermal emission as in a conventional MOSFET instead of direct tunneling as in an SB-CNFET and correspondingly S-values of $\sim$ 60mV/dec are attainable [21].

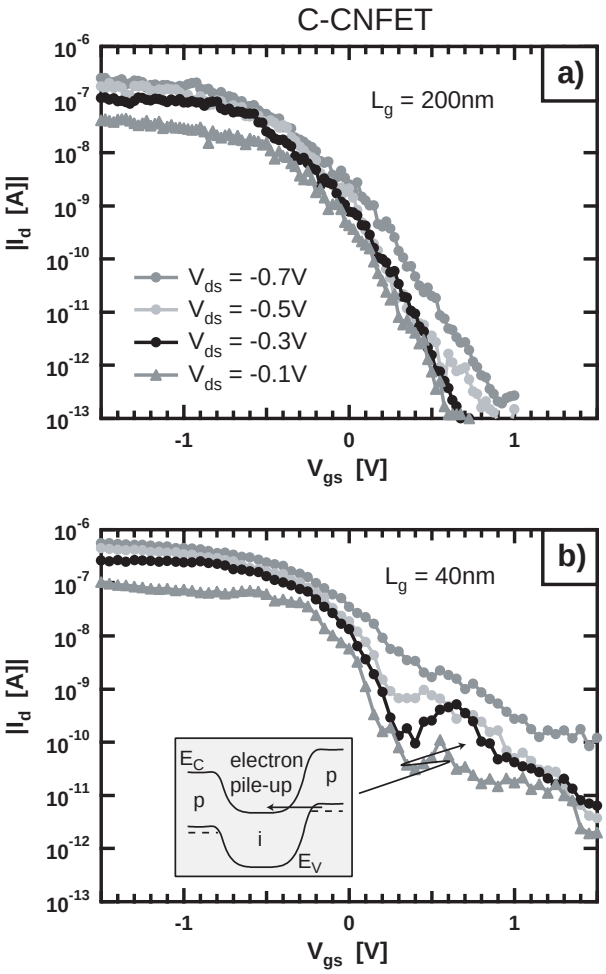

Fig. 3. Experimental results on two C-CNFETs with different gate length of L_g = 200nm and 40nm respectively. The equivalent gate oxide thickness (EOT) is 4nm. In both cases the same drain voltages of -0.1V, -0.3V, -0.5V, and -0.7V were used. The legend for b) is the same as for a). The inset in b) illustrates schematically the situation that is referred to as pile-up in the text.

However, a critical aspect is ignored in these arguments. Indeed, under certain conditions, electron (hole) pile-up occurs in the gated region of the p-type (n-type) C-CNFET [22]. In case of a p-type C-CNFET electrons are injected from the drain side into the gated region and cannot leave the device toward the source (see inset of Fig. 3b). These charges can prevent the gate from effectively moving the bands to turn the device off. The higher the drain voltage the more pronounced the effect. As we show here for the first time, this phenomenon is particularly harmful for transistors that are aggressively scaled in terms of their gate length L_g. In Fig. 3a) and b) experimental characteristics for two different C-CNFETs are presented. While a C-CNFET with an L_g = 200nm shows low off-currents and almost no drain voltage dependence in the subthreshold region of the transistor, a similarly designed device with a gate length of only 40nm on the other hand shows drastically deteriorated off-state performance [23]. Note that the current and gate voltage axes are identical for the two plots. In both cases it is ensured that long-channel type characteristics are obtained by using a 4nm thick aluminum oxide gate dielectric layer. Output characteristics are monitored to verify that a proper current saturation is observed for high enough drain voltages. When L_g decreases so does the capacitance of the island that is formed underneath the gate and the impact of the accumulated charge on the device characteristics increases. The larger the drain voltage the smaller (more negative) the gate voltage for which the subthreshold characteristics starts deviating from the ideal behavior. The inverse subthreshold slope in the pile-up dominated gate voltage range becomes very large and the aggressively scaled C-CNFET behaves like a "leaky" transistor.

Interestingly, it is the same physics aspect that gives rise to both, the particular switching behavior in an SB-CNFET and the pile-up of charge in case of a C-CNFET. In the context of an SB-CNFET, we have pointed out above that a very abrupt band bending occurs. This situation has been described using the expression: "small Schottky barrier width". It is the same phenomenon which allows for the band-to-band tunneling (BTB-tunneling) from the doped nanotube segment into the gated C-CNFET region. Because of the small diameter t_{ch} of a nanotube the gate can strongly affect the bands inside the tube channel resulting in a high tunneling probability for electrons and holes. In case of the SB-CNFET it is the tunneling from the metal contact into the nanotube conduction or valence band. In case of the C-CNFET it is the tunneling through the band gap from the conduction into the valence band and vice versa.

III. Gate controlled tunneling and a novel T-CNFET device layout

So far, we have discussed why the particular tunneling behavior in CNFETs is harmful for aggressively scaled nano-transistors. Now, we want to ask the question, whether it is possible to make use of this property to our advantage. In this context, we recently explored gate controlled tunneling in a C-CNFET in more detail [25]. While electrical characteristics show a monotonic current decrease for increasing gate voltage within a certain V_{gs}-range (see e.g. Fig. 3a), increasing the gate voltage further (making it more positive) results in an abrupt increase of I_d. This situation is illustrated in Fig. 4. For high enough positive gate voltages [21] the conduction band of the gated nanotube segment is pushed below the Fermi level in the highly p-doped source and drain regions of the C-CNFET. Charge that was able to pile-up in the intrinsic nanotube region can now leave the device towards the source by a second band-to-band tunneling process. This opens another channel for

carrier (hole) transport from source to drain and I_d increases abruptly as apparent for $V_{gs} \approx 0$V in Fig. 4. The important finding of this experiment is that in addition to the normal operation of the C-CNFET it is also possible to utilize gate controlled tunneling for switching and that in this way it is possible to achieve S-values smaller than 60mV/dec at room-temperature [25].

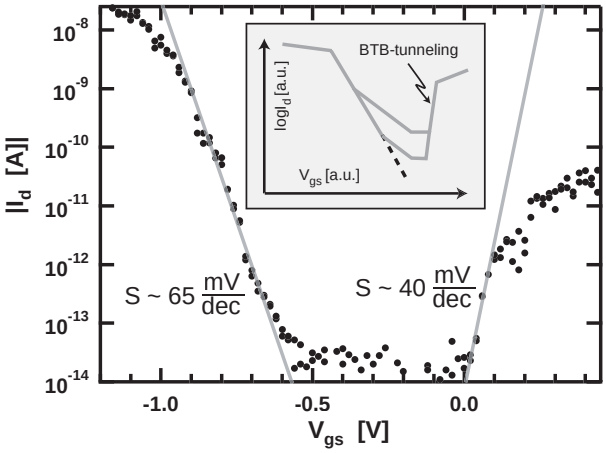

Fig. 4. Subthreshold characteristics of a C-CNFET with $L_g = 200$nm at T=300K for $V_{ds} = -0.5V$. Two subthreshold regions with different S-values are apparent. The steep inverse slope of S$\sim$ 40mV/dec is achieved through BTB-tunneling. The inset shows how characteristics of a device with short L_g would look like for two different drain voltages.

Since the energy gaps of the p-doped and the gated region of the CNFET act as energy filters during the BTB-tunneling process, high energetic carriers in the Fermi distribution are less involved in current flow. By eliminating the high energetic tail of the Fermi distribution, the electronic system gets effectively "cooled down" - the entire system acts like a conventional MOSFET at a lower temperature. While in principle, by utilizing BTB-tunneling, S-values smaller than 60mV/dec are also achievable in silicon MOSFETs [26], experimentally this situation has not yet been realized [27]. On the other hand, carbon nanotubes offer the ideal combination of intrinsic properties to make gate controlled tunneling a viable approach for nano-devices. The important aspects are: 1) ballistic transport in the channel, 2) ultra-small t_{ch} and t_{ox}, 3) small effective masses for electrons and holes, 4) same effective masses of electrons and holes, and 5) a direct energy band gap. While 1) ensures a high current level in the device, 2) to 5) all support a high tunneling probability for the BTB-tunneling process. Moreover, aspects 2) and 3) are the determining factors for the actual value of S as will be discussed below.

In order to make gate controlled tunneling a relevant approach for device applications, it is not enough that an abrupt transition between the transistor on- and off-state can be achieved. It also has to be ensured that high on-currents that translate into a high device performance are obtained at the same time. A C-CNFET is not the right choice in this context. With two BTB-tunneling events involved in the current transport and the aforementioned problem of a distinct drain voltage dependence due to charge pile-up in the gated nanotube area, C-CNFET characteristics would even for ideally scaled conditions exhibit too low current levels and undesirable drain voltage effects. Here we propose for the first time a T-CNFET (see also Fig. 1c) that eliminates all the previously discussed disadvantages of other CNFET layouts and ideally benefits from the concept of gate controlled tunneling discussed before.

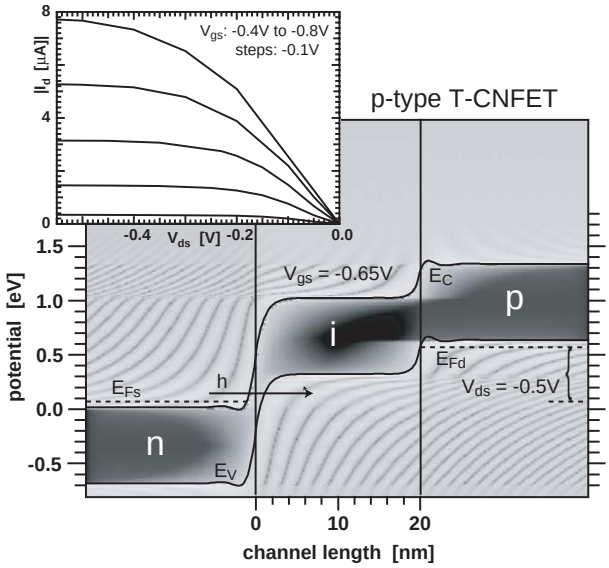

Fig. 5. Conduction and valence band for a T-CNFET according to our simulation at $V_{ds} = -0.5$V and $V_{gs} = -0.65$V. The device is in the on state. The inset shows the corresponding output characteristics of the transistor.

To explain the operation principle of the T-CNFET we will use Fig. 5 that indicates the band bending situation in the on-state of the tunneling device. Fig. 5 is the result of a self-consistent calculation as will be discussed below. The x-axis displays the position inside the nanotube and the y-axis shows the electron/hole energy relative to the conduction band in the n-type region. The plot contains the local density of states information as a gray scale with light and dark areas indicating a high and a low density of states respectively. For negative drain voltage conditions the p-type T-CNFET can be turned on by applying negative gate voltages as for a conventional p-FET. As illustrated in Fig. 5, hole injection from the n-doped source region by tunneling into the intrinsic nanotube segment is enabled by the gate and can be disabled by more positive V_{gs}. The critical BTB-tunneling process occurs at an x-axis value of around zero. Since ballistic transport conditions prevail, this hole current can reach the drain electrode unimpeded. The energy of the holes remains the same throughout the entire nanotube channel and there is no second tunneling barrier to overcome as in the C-CNFET

case. Besides resulting in a higher on-current, this also implies that no charge pile-up can occur in the gated region due to the absence of a cavity-like structure as in the case of a C-CNFET. At the same time inverse subthreshold slopes smaller than 60mV/dec at room-temperature are achievable as discussed in the context of the C-CNFET. Since the drain voltage cannot impact the tunneling probability between the n- and i-region in a well tempered i.e. "long-channel" type transistor, subthreshold characteristics are drain voltage independent as desirable. Another interesting aspect of this device concept is that conventional-looking output characteristic are obtained despite the completely different switching mechanism behind the T-CNFET. Small drain voltage operation is possible as in a regular MOSFET. The inset of Fig. 5 indicates that both a linear and a saturation region exist in the I_d-V_{ds} characteristics of a T-CNFET. The linear behavior for small V_{ds} is a result of the linear increase of open states in the drain region with the drain voltage. Saturation occurs, as in any ballistic MOSFET, due to the exponential decrease of current from the drain to the source for large enough V_{ds} [28]. Last, the same T-CNFET can operate as both an n-type or a p-type tunneling device. By reversing source and drain in Fig. 5 and applying a positive voltage to the n-type part of the tube an n-type T-CNFET is obtained.

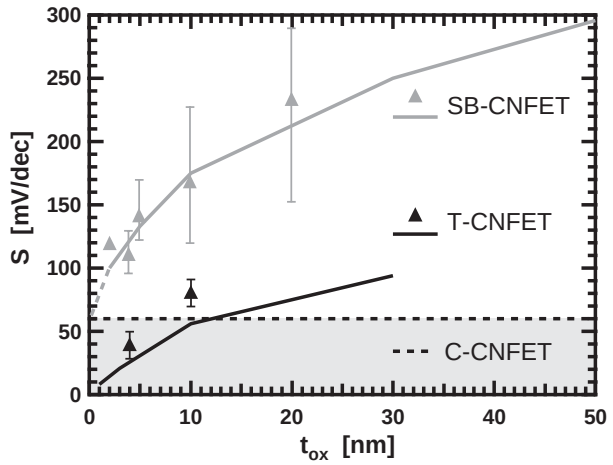

Fig. 6. Experimental results (symbols) and simulations (lines) on the dependence of the inverse subthreshold on gate oxide thickness (t_{ox} = EOT) for the three device concepts under evaluation.

While there are a number of advantages of the T-CNFET, the most appealing aspect is clearly the extremely small S-values that can be obtained. To illustrate this aspect Fig. 6 shows experimental and simulation results (details will be discussed in section IV.) of S as a function of the gate oxide thickness for the various device concepts discussed in this article. As has been pointed out before [20] S varies dramatically with gate oxide thickness for the SB-CNFET due to the strong dependence of the Schottky barrier width at the metal/nanotube interface on the gate field. In fact S is proportional to $\sqrt{t_{ox}}$ [29]. A more detailed analysis [30] reveals that:

$$S \propto \sqrt{m^*_{e,h} \cdot t_{ch} \cdot t_{ox}} \quad (1)$$

Since the Schottky barriers in the contact area are always in series with whatever band bending situation exists for a given gate voltage inside the nanotube channel, S can never be smaller than 60mV/dec for an SB-CNFET. This is not a result of short channel effects due to a diminished gate control. Indeed, for both, the experimental results and the simulations presented here it is ensured that long channel type transistor characteristics are obtained. Consequently, the C-CNFET exhibits a constant inverse subthreshold slope of 60mV/dec in the same plot. The same figure also contains our findings on the T-CNFET. For a nanotube diameter of $t_{ch} = 1$nm and an effective mass of $m^* = 0.1m_0$ S-values smaller than 60mV/dec are predicted for $t_{ox} \leq 10$nm (assuming a dielectric constant of $\varepsilon_r = 4$). The functional dependence of S(t_{ox}) is similar to that of the SB-CNFET with the main difference that $\lim_{t_{ox}\to 0} S = 0$. Note, that eq. (1) holds for the T-CNFET as well. We find that the condition $m^*_{e,h} \cdot t_{ch} \cdot t_{ox} \approx 1$ marks the transition to an S-value smaller than achievable in a conventional MOSFET design. The importance of an ultra-thin body and a thin gate oxide layer becomes apparent from this expression. In addition, Fig. 6 includes two experimental data points for devices operating in the BTB-tunneling regime with gate oxides of $t_{ox} = 4$nm and 10nm respectively. The general agreement with the predicted behavior is apparent and the observed S-values are clearly well below those obtained for the SB-CNFET.

IV. Self-consistent quantum simulation of ultra-thin body devices

In the last paragraphs we started to compare experimental results on carbon nanotube transistors with simulations we have performed using the non-equilibrium Green's function (NEGF) formalism [31]. Our simulations consider a CN-FET consisting of a nanotube in contact with two semi-infinite source/drain metallic contacts. The charge in and current through the CNFET is calculated self-consistently using the NEGF formalism together with a modified 1D Poisson equation due to Young [32] that accounts for the impact of gate oxide thickness and tube diameter on the electrostatics. A quadratic dispersion relation is assumed in the conduction and valence band; the complex band structure in the semiconductor gap is taken into account by an energy dependent effective mass [33]. Transport through the nanotube is treated ballistically. Although our approach simplifies the actual situation e.g. by assuming that the metal contacts behave as ideal conductors with a quadratic dispersion and free electron mass, excellent quantitative agreement between experiment and simulation has been recently demonstrated [25]. This implies that the critical aspects of a CNFET are properly accounted for in our simulation and that it is justified to use our simulation tools to make predictions about more

aggressively scaled nanotube devices than are available to date. It is also possible in this way to perform a more direct comparison of the three device concepts discussed in this article. By utilizing an identical parameter set in terms of geometry and material specific aspects (e.g. effective mass and tube diameter) it is ensured that it is only the device design that results in differences in the transistor performance.

V. Predicted Speed and Power Advantages of T-CNFETs

At this point one may argue that a T-CNFET should always be inferior to a conventional C-CNFET in terms of its on-state performance. Employing tunneling can be expected to reduce the maximum achievable I_{on}-values. The question is whether this can be overcompensated by the steeper inverse subthreshold slope.

To address this issue, we have performed simulations for both types of devices. Figure 7 shows the resulting subthreshold characteristics for moderately scaled CNFETs with gate lengths of $L_g = 20$nm and an equivalent oxide thickness (EOT) of $t_{ox} = 1$nm [34]. As expected higher on-currents can be achieved with the C-CNFET. However, even for rather low drain voltages the p-type C-CNFET shows a substantially deteriorated off-state performance due to electron pile-up in the gated channel region. In fact, at $V_{ds} = -0.6$V the device behaves like a MOSFET exhibiting severe short channel effects (SCEs). As mentioned above, this is a result of two effects, the strong electrostatic control by the gate that allows for injection from the valence band of the p-doped drain region into the conduction band of the gated channel region as illustrated in the inset of Fig. 3b and the small L_g assumed here. From our simulation for $V_{ds} = -0.4$V it is more obvious that the device indeed first shows a conventional switching with an inverse subthreshold slope of $S = k_B T/q \cdot \ln 10$ between -0.4V and -0.1V before pile-up becomes relevant for $V_{gs} \geq -0.1$V.

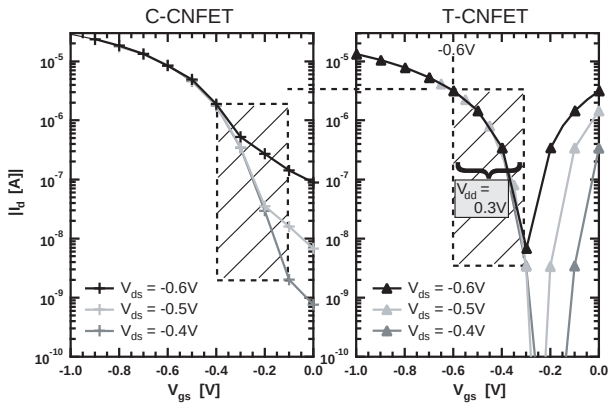

Fig. 7. Simulated performance of a C-CNFET and a T-CNFET for various drain voltages. The parameter set used for both calculations is: $E_g = 0.7$eV, $t_{ox} = 1$nm, $t_{ch} = 1$nm, L_g=20nm, $m^* = 0.1m_0$, and T=380K.

On the other hand, the p-type T-CNFET characteristics for the same drain and gate voltage range show a quite different behavior. The first thing to notice is a distinct drain voltage dependence that resembles the one presented in the context of an SB-CNFET in Fig. 2. While for the left - p-type - branch the aforementioned steep switching behavior due to BTB-tunneling with no particular drain voltage dependence is observable as desired, we notice that the T-CNFET exhibits a clear n-type branch as well. The increase of I_d for large enough positive gate voltages is a result of BTB-tunneling on the drain side of the transistor. The characteristics of a T-CNFET are those of an SB-CNFET but with much steeper inverse subthreshold slope (see Fig. 6) and higher I_{on}/I_{off}-ratio. Also notice, that the value of S in case of a T-CNFET does not deteriorate with increasing temperature [35]. While both, the SB-CNFET and the C-CNFET exhibit S-values proportional to temperature in the relevant T-range for transistor operation between 300K and 380K, S is temperature independent for a T-CNFET. This means that high temperature operation has no negative impact on the device characteristics of a T-CNFET.

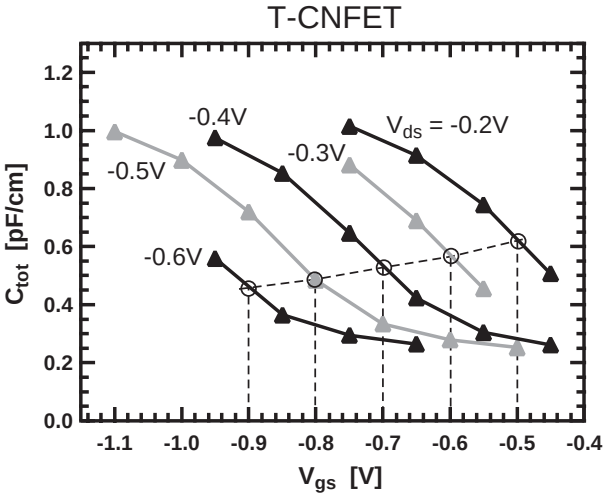

Fig. 8. Total capacitance $C_{tot} = (1/C_g + 1/C_q)^{-1}$ for the T-CNFET in Fig. 7 as a function of gate voltage for various applied drain voltages.

We now want to quantify the performance advantages of a T-CNFET in comparison with a C-CNFET taking into account all of the above effects. A metric to characterize the switching speed in a device is the gate delay $\tau = C_{tot} \cdot V_{dd}/I_d$ for a given I_{on}/I_{off}-ratio. Here C_{tot} includes contributions from the geometrical gate capacitance C_g and the quantum capacitance C_q of the nanotube (see also [36], [37]). Since carbon nanotubes are effectively one-dimensional (1D) conductors, the relatively small 1D-density of states $D_{1D}(E)$ allows to experimentally realize C_g-values that are comparable to C_q which is proportional to $D_{1D}(E_F)$. Because of this situation the quantum capacitance cannot be ignored in a scaled CNFET [38]. What makes the situation complicated is that C_q also depends on the coupling $T(E_F)$ between the contacts - the

electron (or hole reservoirs) - and the gated channel region [30] and in addition on the drain and the gate voltage.

Figure 8 illustrates how C_{tot} changes for the T-CNFET considered here as a function of drain and gate voltage. The first aspect to notice is that C_{tot} is indeed not a constant even well above the threshold voltage (for $V_{gs} \leq -0.45V$) as would be the case in a conventional MOSFET device. In fact, the total capacitance increases by a factor of four from its minimum value with decreasing (more negative) gate voltage and increasing (more positive) drain voltage. These trends can be qualitatively understood as follows: Making V_{gs} more negative increases the transmission $T(E_F)$ of holes from the n-doped source region of the T-CNFET into the gated channel region. Since $C_q \sim T(E_F)$ [30] this increases the quantum capacitance and thus the total capacitance $C_{tot} = (1/C_g + 1/C_q)^{-1}$. On the other hand, making V_{ds} more negative reduces the amount of charge injected from the drain side. As discussed above, this is also the reason for the saturation of I_d as a function of V_{ds}. Consequently, the quantum capacitance decreases and C_{tot} accordingly.

For our analysis we use the C_{tot}-value that corresponds to the applied voltage conditions. E.g. for an I_{on}/I_{off}-ratio of 1000, at $V_{dd} = |V_{ds}| = 0.3V$ the gate voltage is $V_{gs} = -0.6V$ as apparent from the marked area in Fig. 7 for the T-CNFET. Using Fig. 8 we find $C_{tot}(V_{dd} = 0.3V) \approx 0.57$pF/cm. The dashed line and hollow circles in Fig.8 denote the trend of C_{tot} with V_{dd}. The larger V_{dd}, the smaller the total capacitance of the system - which implies that the drain voltage has a stronger impact on the total capacitance of the system than the gate voltage under the conditions considered here.

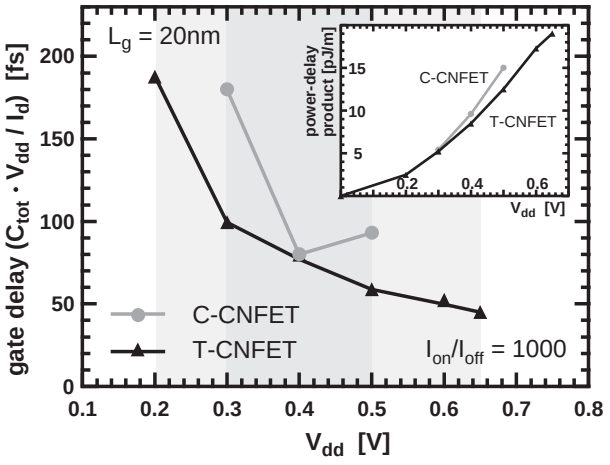

Fig. 9. Gate delay τ for the C-CNFET and the T-CNFET discussed in Fig. 7. Superior device characteristics are obtained for the T-CNFET for any V_{dd}. The inset shows the power-delay product for both device layouts.

By performing the type of analysis described above for both, the T-CNFET and the C-CNFET, we are able to evaluate the gate delay τ as a function of V_{dd} at a fixed I_{on}/I_{off}-ratio of 1000 [39]. Fig. 9 illustrates our findings for a bias ranging from 0.1V to 0.8V. We notice that the T-CNFET shows the expected monotonic behavior of τ as a function of V_{dd}. As in a conventional MOSFET, the ratio V_{dd}/I_d is not a constant and consequently the gate delay improves for increasing V_{dd}. However, there is a finite size V_{dd}-window that allows for CNFET operation. Since we claimed an I_{on}/I_{off}-ratio of 1000, a drain voltage above 0.65V cannot be used. As discussed in the context of Fig. 7, the off-current of the T-CNFET is strongly drain voltage dependent and deteriorates for increasing V_{ds}. At the low V_{dd} side, the steep inverse subthreshold slope allows for excellent device performance even at a supply voltage of only $V_{dd} = 0.2V$.

On the other hand, the situation in the C-CNFET is characterized by a much smaller V_{dd}-window. Due to the above discussed charge pile-up, the C-CNFET fails to support an on-/off-current ratio of 1000 for V_{dd}-values above 0.5V. Below around $V_{dd} = 0.3V$ the inverse subthreshold slope limits the use of the C-CNFET for T=380K. Interestingly, the gate delay is always larger for the C-CNFET despite the higher absolute on-current value shown in Fig. 7. There is a twofold reason for this behavior: First, The better S-value of a T-CNFET results in a higher on-current for most V_{dd}. This is illustrated in Fig. 7 for $V_{dd} = 0.3V$ by the shaded areas and the dashed lines. Second, the smaller quantum capacitance [30] in the T-CNFET due to the tunneling process involved in the on-state characteristics results in a reduced total capacitance. Both effects improve the gate delay in the T-CNFET relative to the C-CNFET.

Even for a V_{dd} of 0.4V where both devices show the same gate delay, the T-CNFET is the superior device concept. Due to the smaller total capacitance, the power delay product which is plotted in the inset of Figure 9 always exhibits a smaller value for the T-CNFET than for the C-CNFET.

VI. Summary

The chain of arguments presented in this article can be summarized as follows: To increase the performance of an FET, short gate lengths L_g and high mobilities are required. Since nanotubes typically exhibit very small diameters they allow for excellent gate control while not suffering from mobility degradation. This is the key to an aggressive L_g-scaling. However, ultra-thin body devices - as CNFETs - always show an increased probability for tunneling processes. Charge pile-up does not allow to employ well established device concepts similar to those of conventional n- or p-type MOSFETs in this case. Instead, it is required to transition from a device that operates based on the gate control of a thermal emission current to a gate controlled tunneling device. We have shown that this transition is not only necessary but actually also beneficial for the overall device performance in terms of switching speed and power consumption by introducing the T-CNFET.

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