ECS Transactions, 28 (5) 3-13 (2010)
10.1149/1.3367931 ©The Electrochemical Society

Graphene RF Transistor Performance

K. A. Jenkins, Y.-M. Lin, D. Farmer, C. Dimitrakopoulos, H.-Y. Chiu, Alberto Valdes-Garcia, Ph. Avouris, and A. Grill

IBM T. J. Watson Research Center, Yorktown Heights, NY 10598

Recent excitement about graphene as a possible material for high-frequency electronics has lead to demonstrations of high-frequency field-effect transistors (FETs) in the last two years. Although graphene FETs operate by a different principle than silicon MOSFETs, and have different DC characteristics, their ac properties are quite similar. Hence the high intrinsic mobility of graphene leads to the expectation of high frequency operation of gated graphene FETs. Demonstrations of frequency response in the GHz regime have been shown using both exfoliated flakes and synthesized graphene. An intrinsic cut-off frequency as high as 100 GHz has been achieved in a 240-nm-gate graphene FET fabricated on a 2" wafer of epitaxially-grown graphene. This value exceeds that of Si MOSFETs at the same gate length, illustrating the potential of graphene for RF applications.

Introduction

Graphene has recently generated a great deal of excitement as a material for high-performance microelectronics. It is a two-dimensional (2D) material, consisting of a sheet of carbon atoms arranged in a honeycomb lattice, weakly bound to a supporting substrate. While there has been enormous research activity on graphene based on its many unusual physical properties, it is primarily considered a very promising candidate for high-performance devices due to its exceptional electrical properties: it has a high intrinsic carrier mobility (greater than 10,000 cm^2/Vs at room temperature) (1) and a large saturation velocity (~ 5.5×10^7 cm/s) (2), both which greatly exceed the corresponding values of silicon. Thus there is a real possibility that graphene transistors will operate at high frequency, which can be exploited to fabricate correspondingly high frequency RF circuits, such as low-noise amplifiers and power amplifiers. Furthermore, the ultra-thin body thickness of graphene offers ideal two-dimensional electrostatics for the ultimate scaled-down device.

While single-layer graphene was first successfully isolated and identified by micromechanical exfoliation of bulk graphite (3,4), different synthesis approaches have also been developed and realized, such as sublimation of Si from silicon-carbide (SiC) substrates (5) and chemical vapor deposition (CVD) on metal films (6,7), to produce large-area or even wafer-scale graphene layers. The rapid advances in synthesis, together with its outstanding electrical properties, have opened up practical opportunities for circuits and applications based on graphene, and made it one of the most promising materials in emerging technologies. With recent progress in wafer-scale graphene synthesis, there is now the possibility of patterning it using many of same lithographic and processing equipment using for silicon technology, to form high-performance integrated RF circuits.

Recently, graphene FETs with cut-off frequencies in the GHz regime have been reported by several groups (8-10). This paper reviews the progress in fabricating, measuring, and modeling of graphene FETs for high-frequency electronics, reports graphene devices with cut-off frequencies (f_T) up to 100 GHz, and compares some the electrical characteristics of graphene FETs with silicon MOSFETS at similar dimensions.

Fabrication of Top-gated Graphene FETs

Most of the experimental knowledge of graphene's electrical properties has been acquired by using simple bottom-gated devices. The graphene is placed on silicon or other semiconducting wafer having a thin oxide layer, and metallic terminals are deposited on the graphene. The wafer is biased from its back to provide a gate voltage (or field) on the graphene. However, practical devices and circuits require a small top gate, just as in conventional integrated circuits. This is particularly required for RF devices, for which the best substrates are insulating. Recently there has been increasing emphasis on forming this top gate and its corresponding dielectric layer, resulting in FETs which structurally resemble conventional top-gated MOSFETs.

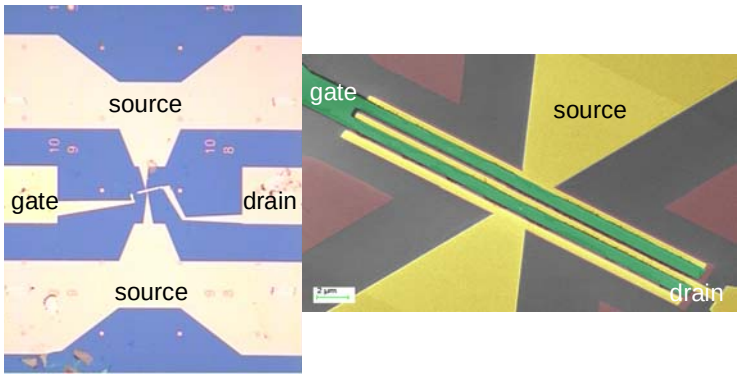

Figure 1. Optical (left) and SEM (right) micrographs of graphene FETs for high frequency measurements, made with exfoliated flakes and epitaxial graphene, respectively.

Fig. 1 shows micrographs of top-gated graphene transistors with layouts required for high-frequency measurements. On the left, a single layer graphene was prepared by mechanical exfoliation. After identification of a suitable flake of graphene, the source and drain electrodes, made of Pd/Au metals, were fabricated by e-beam lithography and lift-off. A layer of 12-nm Al_2O_3, formed by ALD (atomic layer deposition), was deposited as the top-gate dielectric, and a customized gate metal stack was deposited as the top-gate electrode. On the right, the device was formed on epitaxially grown graphene on a SiC wafer. Whereas exfoliated flakes require custom layouts to conform to the size and placement of the flakes, wafer-scale graphene allows simple, regular structures, similar to those employed in silicon technologies.

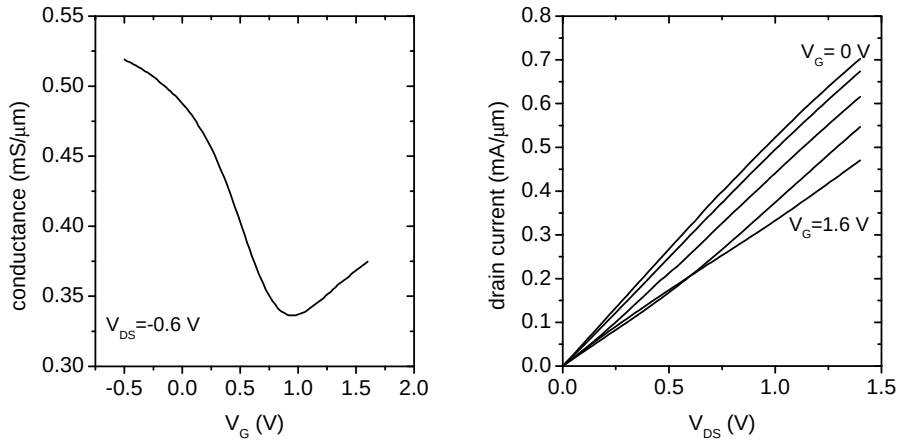

Figure 2. Typical conductance (left) and output characteristics (right) of a graphene FET.

Typical DC conductance and output characteristics of graphene FETs are shown in Fig. 2. The conductance characteristics exhibit a "V" shape behavior, reflecting the ambipolar transport in graphene. It has been shown that after subtracting the series resistance that consists of contact resistance and the resistance of the un-gated graphene regions, the channel conductance is linearly dependent on gate voltage.

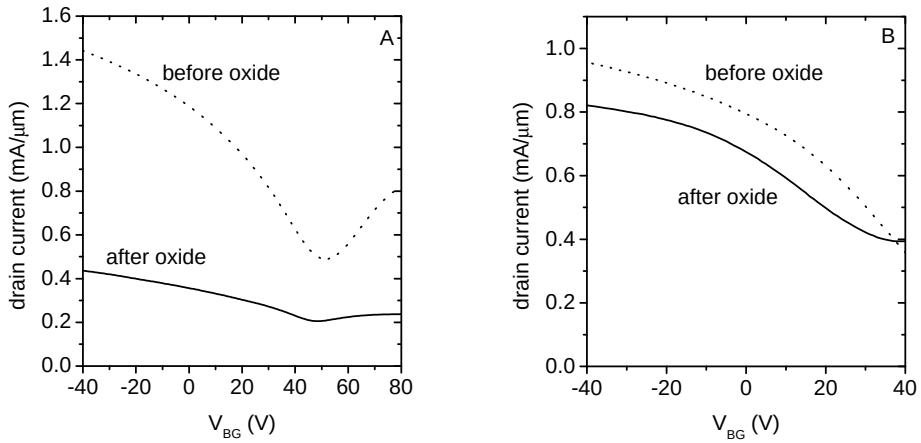

Figure 3. Comparison of conductance of graphene processed with two different top gate dielectrics. Dashed line: conductance before dielectric deposition; solid line: after dielectric deposition.

In such top-gated graphene FETs, device performance is primarily limited by the mobility degradation of graphene during the device fabrication process, particularly after oxide deposition, and a significant series resistance compared to channel resistance. For example, Fig. 3 compares the conductance characteristics of two graphene FETs before and after the oxide deposition with two different deposition processes. In process A, the graphene surface is first functionalized with NO_2 to promote the uniform oxide coverage in the subsequent ALD process of Al_2O_3. In process B, a layer of 2-nm naturally-oxidized

Al_2O_3 is used prior to ALD (11). The conductance curves were obtained by applying a back-gate bias while the top gate was unconnected, hence the different response is just due to the effects of the gate dielectric process. It is found that process B better maintains the intrinsic transport properties of graphene by improving the interface between graphene and the oxide. To take advantage of the high mobility of intrinsic graphene for transistors, it is critical to develop a robust gate oxide process which does not degrade the mobility.

Electrical Characteristics of Graphene FETs

DC Characteristics

Graphene transistors differ from silicon MOSFETs in several significant ways. Graphene is a zero-bandgap semiconductor, unlike silicon, GaAs or InP. Its conductance is modulated by a change in the density of states, not by the creation of an inversion layer, and the graphene channel can not be doped by substitution, but rather by surface doping. Both holes and electrons are massless and have about the same velocity in the channel region. These differences lead, of course, to very different electrical characteristics: the conduction is ambipolar, the on-off ratio is very small, and the output characteristic may not show saturation.

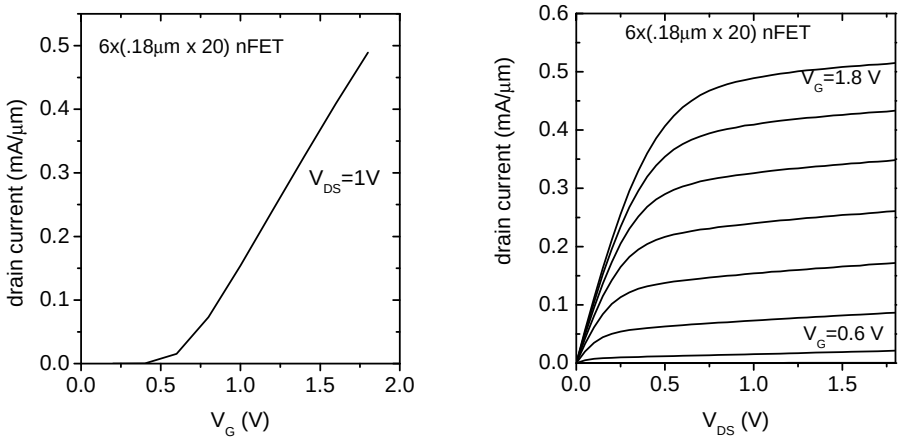

Figure 4. Typical conductance (left) and output characteristics (right) of a silicon MOSFET.

Examples of typical MOSFET behavior are shown in Fig. 4, which can be compared to the graphene behavior above (Fig. 2). However, in spite of the differences, the fact that a gate voltage does modulate the drain current leads to the possibility of graphene FETs as a high frequency amplifying device. The small on-off ratio achieved at present prevents the immediate use of graphene for VLSI digital transistors, but since RF circuits are essentially always on, this is not major problem, and it is in the realm of RF circuits that graphene transistors will likely see their first practical use.

High-Frequency Properties

Although the DC characteristics of silicon and graphene FETs are quite different, the small signal AC behavior of graphene devices is similar in many respects.

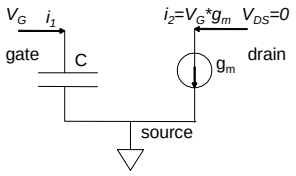

Figure 5. Simple model to describe small signal behavior of FETs.

The most basic equivalent small-signal circuit of an FET is shown in Fig. 5. The circuit illustrates an input capacitance corresponding to the gate, and a transconductance element corresponding to the voltage-controlled modulation of the current through the device channel. From this simple circuit, two important equations are easily obtained. Defining the small signal current gain, $h_{21,}$ as the ratio of the output current to the input current, i_2/i_1,

$$|h_{21}| = f_T/f$$
$$f_{T=} g_m/2\pi C$$

where f is the frequency of the signal applied to the gate, i_2 is the output AC drain current, and i_1 is the AC gate input current, g_m is the transconductance and C is the input capacitance. f_T is defined as the frequency at which $|h_{21}|$ becomes 1, and is known as the cutoff frequency. The first equation describes the frequency roll-off of current gain at a fixed DC bias, and the second relates cutoff frequency to the DC transconductance and the gate capacitance which the input signal drives. Cutoff frequency is a physically significant figure of merit to gauge performance of transistors, as it indicates the maximum frequency with which a signal can propagate through the device.

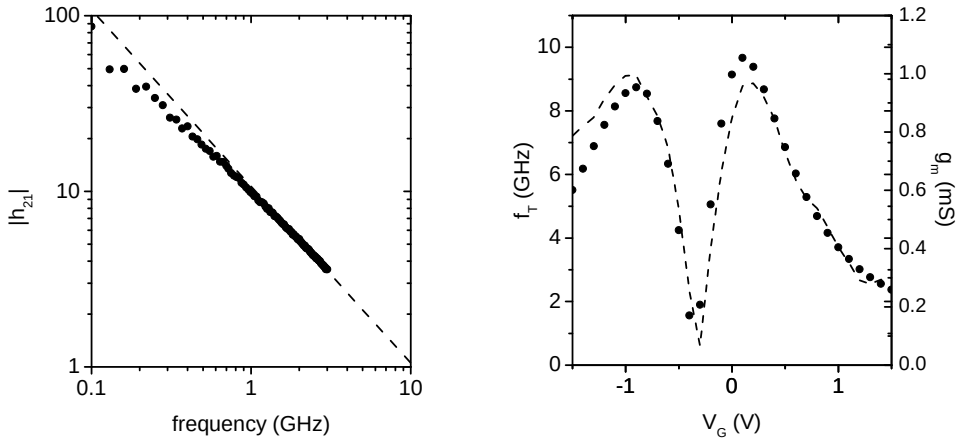

Figure 6. (Left) Example of current gain, $|h_{21}|$, of an exfoliated-graphene FET, showing *1/f* dependence. (Right) Measurements showing that f_T (dots) and g_m (dashed line) are proportional for a graphene FET.

Both of these properties are exhibited by graphene transistors. An example of the *1/f* behavior at a single bias point is shown in Fig. 6a. It is seen that the current gain, $|h_{21}|$, follows *1/f* exactly, so that cutoff frequency is a well-defined term. The h_{21} parameter is obtained from measurements of s-parameters, using a vector network analyzer. Using well-established techniques, the effect of the parasitic capacitance, resistance, and inductance of the probe pads connecting to the device is removed by measuring special "open" and "short" structures and de-embedding the intrinsic device s-parameters using these measurements. The s-parameters are then converted to any other parameter set, such as h-parameters, through a linear transformation.

The relationship between cutoff frequency and transconductance is illustrated in Fig. 6b. This example uses exfoliated graphene flakes, but the same result is obtained with epitaxially-grown graphene. Even though transconductance as a function of gate voltage of graphene FETs is very different from that of silicon MOSFETs, its relationship to cutoff frequency is still correct. Thus, the basic concept of an RF graphene FET is demonstrated with these two observations. This leads the way to developing more precise models which can be used to optimize device structures and which can be used for designing circuits with graphene FETs.

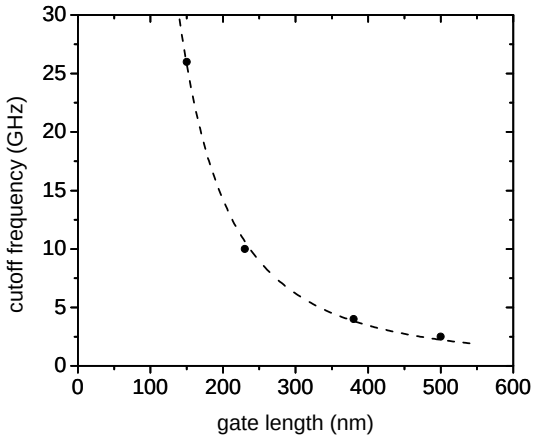

Figure 7. Measurement of the gate length dependence of the cutoff frequency of FETs fabricated with exfoliated graphene flakes.

An additional interesting fact to compare with silicon MOSFETs is the relationship between cutoff frequency and gate length. Traditional long-channel MOSFETs have the cutoff frequency increasing as $1/L_G^{2.}$ However, with channel length scaling to the sub-micron regime, this has changed for short-channel devices, to a $1/L_G$ dependence. Measurements with graphene FETs on exfoliated flakes are shown in Fig. 7, and indicate a $1/L_G^2$ dependence. Although this may not be true for all graphene devices, it does suggest that a figure of merit like f_T*L_G may not be appropriate, and that actual performance at some gate length can not safely be predicted by length scaling.

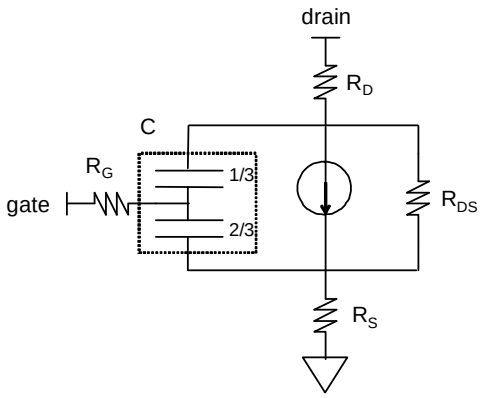

Figure 8. Small signal model of graphene FETs.

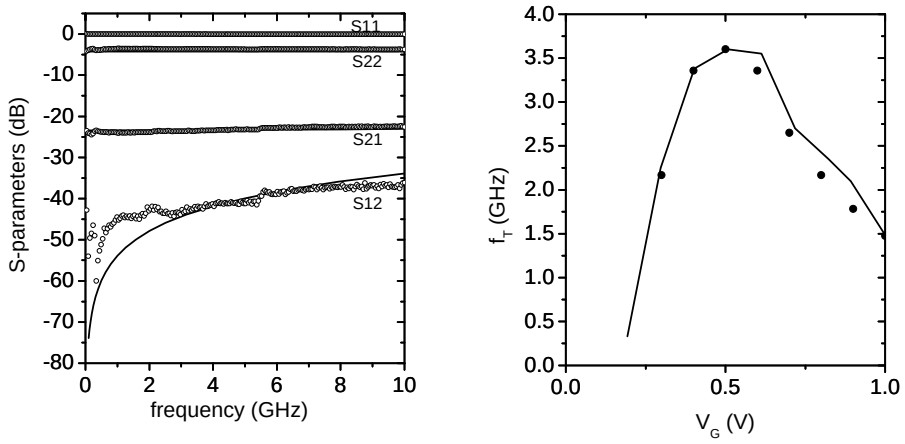

Figure 9. (a) Comparison of s-parameters from the model shown in Fig. 8 with the measured s-parameters of a graphene FET; (b) comparison of modeled f_T with measurements, as a function of gate voltage.

Starting with the basic FET model of Fig. 5, a more precise device model has been developed which takes into account the physical structure of graphene transistors (12). The model is shown in Fig. 9. It contains the basic elements as above, but also adds gate resistance (R_G), source and drain contact and access resistances (R_S and R_D), which though physically distinct, can be lumped into single components, and source-to-drain conductance ($1/R_{DS}$). The validity of this model has been demonstrated by finding numerical values for the parameters so as to match modeled s-parameters with the measurements. An example fit to the s-parameters using such a model is shown in Fig. 9a. An excellent match of the s-parameters is found up to the cutoff frequency, 4 GHz, of the device modeled. Furthermore, by matching the model s-parameters, and using the measured transconductance, the model also correctly predicts the cutoff frequency as a function of gate voltage, as shown in Fig. 9b (12).

The additional resistances and conductance required to model the fabricated device which are shown in Fig. 9 give important insights into how to optimize the frequency response of a graphene FET. For example, it is easily seen that the source resistance reduces the effective transconductance, g_m, and hence, reduces the f_T. Similarly, the presence of the low output resistance, R_{DS}, (which would ideally be infinite) divides the generated current so that less is available at the drain, also reducing cutoff frequency. Engineering solutions to reduce these resistances should result in a higher frequency device.

A demonstration of this analysis was shown using exfoliated graphene in (13). In this example, the devices were built on high-resistivity silicon substrates with an Al_2O_3 gate oxide. It was recognized that the access resistance, due to the ungated graphene, was limiting the cutoff frequency, but by applying a back bias via the substrate while simultaneously applying the top gate bias, the access resistance could be reduced by electrostatic doping. In this way, a cutoff frequency of 50 GHz was achieved with a device with a 350nm gate length, greater than the cutoff frequency of a silicon nFET of the same gate length. This points to the importance of engineering a device which minimizes this resistance. Similarly, reduction of the contact resistance will further increase transistor speed and power gain.

High-Frequency Graphene FETs on Wafer-Scale Synthesized Graphene

To build integrated RF circuits, however, requires uniform wafer-scale graphene, as a starting material, with high mobility, followed by the same considerations for gate dielectrics and device optimization. Recent work has shown significant progress toward this goal. Different synthesis approaches have also been developed and realized, such as sublimation of Si from SiC substrates and CVD on metal films, to produce large-area and even wafer-scale graphene layers (5-7).

Moon et al (9) reported a graphene FET using epitaxially-formed graphene with a cutoff frequency of 4.4 GHz for a 2 μm channel device, making a cutoff frequency-gate length product (f_T*L_G) 8.8 GHz-μm, which is very similar to the value of short-channel silicon nFETs.

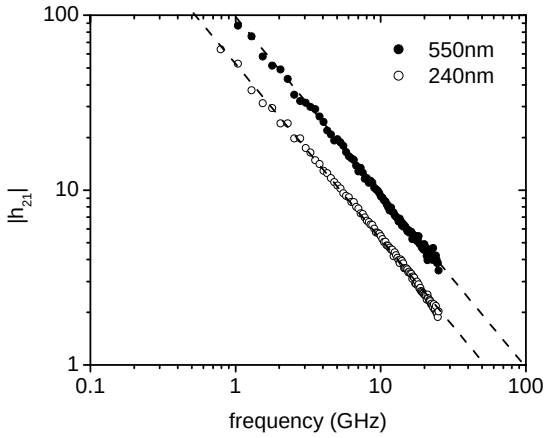

Figure 10. Measurements of a graphene FET demonstrating a cutoff frequency of 100 GHz.

Recently, graphene FETs built at IBM with epitaxially-grown graphene on SiC have been shown to exceed cutoff frequency of silicon nFETs of comparable channel length A cutoff frequency as high as 100 GHz for a device with a gate length of 240nm is shown in Fig. 10(14). A device with a gate length of 550nm on the same wafer had a cutoff frequency of 53 GHz. In this case, graphene was grown epitaxially on high-purity semi-insulating 2" SiC wafer, followed by deposition of a novel buffered gate electrode which does not degrade the mobility of the grown graphene (15,16). The semi-insulating SiC substrate is ideal for low-loss integrated RF circuits.

In many real application circuits, power gain is an important figure of merit, since delivering power to a load which is generally required of an RF circuit. To assess the performance of graphene in this regard, a power gain figure of merit, f_{max}, is generally used. Unlike cutoff frequency, there are many definitions of power gain, and no universal definition is used by all authors.

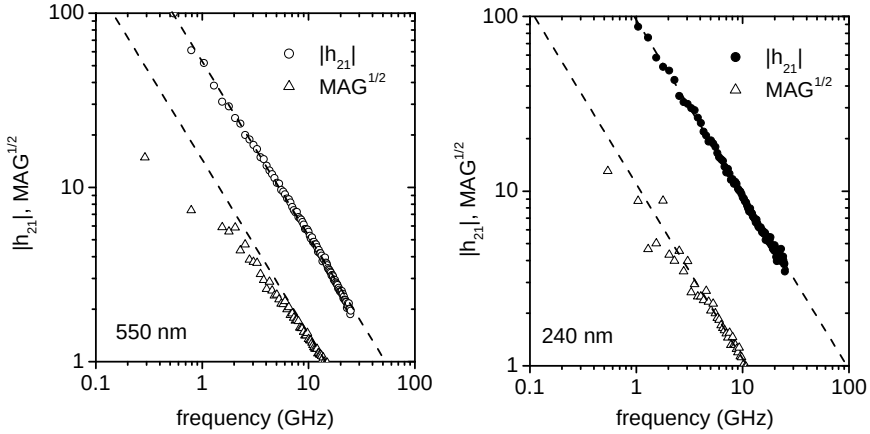

Figure 11. Measurements of power gain and current gain of the two graphene FETs of Fig 10.

Two examples of f_{max} measurements are shown in Fig. 11 along with the f_T measurements of Fig. 10. The maximum available gain, MAG, is obtained directly from s-parameters, but is understood to be related to the device structure as explained above. A properly behaved FET exhibits MAG falling as $1/f^2$, as seen in this plot. This means that f_{max} is well defined. It is seen that that f_{max} does not scale with gate length, as does f_T. This maximum frequency is related to cutoff frequency, but is also affected by the input and output impedance of the device. The input impedance is predominantly affected by the resistance of the gate electrodes, which is, in turn, determined by the geometric layout of the device. The output impedance is determined by the source-to-drain conductance (R_{DS} in Fig. 8), which is more related to the channel electrical properties than it is to layout. It is noted that these devices were not optimized to reduce gate resistance.

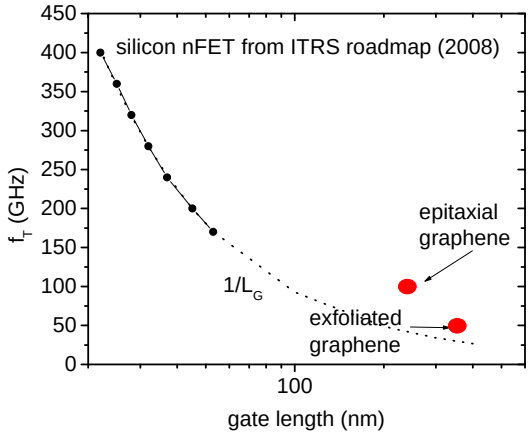

Figure 12. Comparison of the present frequency performance of graphene FETs with silicon FETs as a function of gate length.

To compare the present state of RF performance of graphene transistors to silicon technology, it is useful to use the reports of the International Technology Roadmap for Semiconductors (ITRS) (17). Two cutoff frequency achievements by the IBM team are compared with silicon nFETs in Fig. 12. On this graph are plotted the frequency expected as a function of gate length, as given by ITRS. Two graphene FETs are also plotted as a function of gate length, and it is seen that both the exfoliated device and the epitaxial devices are faster than silicon FETs at the same gate length. As it is known that the graphene mobility in these devices is still far below that which can be obtained when it is isolated by suspension, there is great potential for achieving devices faster than silicon without aggressive channel length scaling.

Although these high frequency FETs have been achieved in very short time, there is still a potential for much faster devices which requires continual improvement in the factors presented here. In addition, most of the present demonstrations have not addressed the question of achieving high frequency power gain. While this requires high cutoff frequency, it also requires significantly decreasing the basic output conductance of submicron devices, and, eventually, utilization of multiple metal connections to optimize input gate resistance.

Summary

Rapid advances in fabricating graphene FETs in the last few years have raised the significant possibility that they might be useful as high frequency devices. Moving from the early studies of their DC characteristics using back gate biasing, a number of RF devices, using top-gating, have been published. The highest cutoff frequency reported to date is 100 GHz, obtained with an FET having a gate length of 240nm. This frequency is higher than the frequency of a silicon nFET of the same dimension. The best frequency responses have been obtained on graphene synthesized on insulating SiC substrates, opening the possibility of integrated RF circuits.

Acknowledgements

This work is supported by DARPA under contract FA8650-08-C-7838 through the CERA program. The views, opinions, and/or findings contained in this article/presentation are those of the author/presenter and should not be interpreted as representing the official views or policies, either expressed or implied, of the Defense Advanced Research Projects Agency or the Department of Defense. Approved for Public Release, Distribution Unlimited.

The authors are grateful to C.-Y. Sung for his leadership and management of this work.

References

1. K. I. Bolotin *et al., Solid State Comm*, **146**, 351 (2008).
2. I. Meric *et al., IEDM Digest* 4796738, (2008).
3. K.S. Novoselov, et al., *Nature*, **438**, 197 (2005).
4. Y. Zhang, Y.-W. Tan, H.L. Stormer, P. Kim, *Nature*, **438**, 201 (2005).
5. C. Berger, *Science*, **312,** 1191 (2006).
6. A. Reina et al., *Nano Letters*, **9**, 35 (2009).
7. K.-S. Kim et al., *Nature*, **457**, 706 (2009).
8. Y.-M. Lin et al, *Nano Letters*, 2009, **9,** 422, (2008).
9. J. S. Moon *et al., IEEE Electron Device Letters*, **30**, 650 (2009).
10. I. Meric et al., IEDM Digest 4796738 (2008).
11. S. Kim *et al*., *Appl. Phys. Lett*., **94**, 062107 (2009).
12. A. Valdes-Garcia *et al*, manuscript in preparation.
13. Y-M. Lin *et al.,* IEEE *Electron Device Letters,* **31**, 68 (2010).
14. Y-M Lin *et al., Science* **327**, 662 (2010).
15. D. B. Farmer et al, *Nano Letters* **9**, 4474 (2009).
16. C. Dimitrakopoulos *et al*, to be published
17. http://www.itrs.net/Links/2008ITRS/Home2008.htm