High-Performance Dual-Gate Carbon Nanotube FETs with 40-nm Gate Length

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***Abstract*—We report on a high-performance back-gated carbon nanotube field-effect transistor (CNFET) with a peak transconductance of 12.5 μS and a delay time per unit length of $\tau/L = 19$ ps/μm. In order to minimize the parasitic capacitances and optimize the performance of scaled CNFETs, we have utilized a dual-gate design and have fabricated a 40-nm-gate CNFET possessing excellent subthreshold and output characteristics without exhibiting short-channel effects.**

***Index Terms*—Carbon nanotube (CN), dual gate, field-effect transistor (FET), short-channel effect.**

I. Introduction

Carbon nanotubes (CNs) are promising candidates for post-Si nanoelectronics [1]. They are particularly attractive for high-speed applications due to their quasi-ballistic properties [2], [3] and high Fermi velocity ($\sim 10^6$ m/s) [4]. The small-signal switching speed of a transistor is characterized by the intrinsic delay time $\tau = 2\pi C_G/g_m$, where C_G is the gate capacitance and $g_m = dI_d/dV_{\rm gs}$ is the transconductance. While τ is reduced with decreasing gate length L as desirable, care must be taken when scaling devices in order to maintain the desired transistor characteristics.

In this letter, we report on a high-performance carbon nanotube field-effect transistor (CNFET) with a delay time per unit length of 19 ps/μm, the smallest value reported for CNFETs to date. In order to further minimize the parasitic capacitances, we exploit a dual-gate structure and fabricate a 40-nm-gate CNFET possessing excellent subthreshold and output characteristics. To our knowledge, this is the shortest gate length that has been demonstrated for a CNFET without short-channel effects so far.

II. Back-Gated CNFET

The schematic device structure of the back-gated CNFET is depicted in the inset of Fig. 1(a). The nanotubes used here are produced by arc discharge [5] and possess an average diameter of $D \sim 1.8$ nm. Two Pd contacts form the source and drain, and p-doped Si substrate is used as the gate. Pd is used here to minimize the Schottky barrier height for hole carriers at the metal/nanotube contacts [6]. Fig. 1(a) and (b) shows the output and subthreshold characteristics of the back-gated CNFET device measured at room temperature, respectively. The CNFET possesses a subthreshold swing $S = 140$ mV/dec with an $I_{\rm ON}/I_{\rm OFF}$ ratio $\geq 10^5$ and exhibits output characteristics similar to those of a regular p-MOSFET.

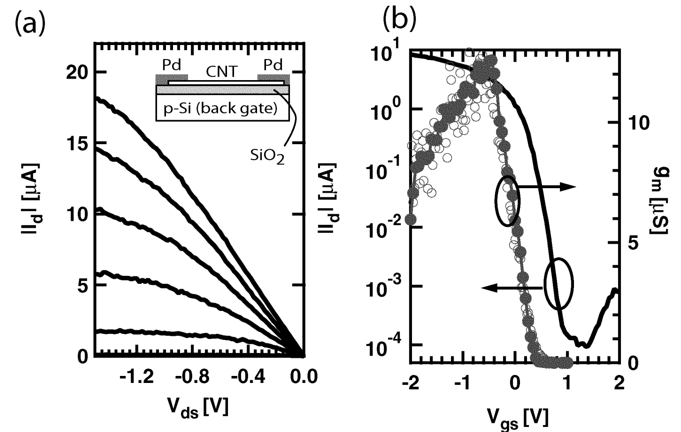

Fig. 1. (a) Output characteristics of a back-gated CNFET for gate voltages $V_{\rm gs} = -1.6$ V to 0.4 with a 0.4 V step. The inset shows a schematic diagram of the device structure. The oxide thickness is 10 nm, and the source/drain contacts are made of 40-nm-thick Pd with a separation of 600 nm. (b) Subthreshold characteristics of the CNFET at $V_{\rm ds} = -0.5$ V. The transconductance g_m for $V_{\rm ds} = -1.5$ V measured at 300 K (open circle) and 90 K (closed circle) are shown with respect to the right axis.

Fig. 1(b) also shows the CNFET transconductance g_m for $V_{\rm ds} = -1.5$ V measured at two temperatures: $T = 90$ K (closed circle) and 300 K (open circle). We note that for $-1.5\ {\rm V} \leq V_{\rm ds} \leq 0$ V, the measured currents I_d of the CNFET are nearly identical between the two temperatures, indicating a carrier mobility independent of T and device reliability over a wide temperature range. In the low-bias regime, the T-independent mobility results from the quasi-ballistic transport because the channel length (600 nm) is much shorter than the electron mean-free path associated with acoustic phonon scattering in carbon nanotubes (≥ 1.6 μm [3], [7]). On the other hand, the transport in the high-bias regime is dominated by optical phonon scattering that is a T-independent mechanism. Thus, the scattering rates as well as the mobility of the CNFET are temperature independent in the entire bias regime.

In Fig. 1(b), the transconductance of the CNFET exhibiting a peak value of $g_m \sim 12.5$ μS at $V_{\rm gs} \sim -0.5$ V. To calculate the gate delay of the CNFET, the gate capacitance C_G is derived by $C_G^{-1} = C_{G,{\rm ox}}^{-1} + C_{G,q}^{-1}$, where $C_{G,{\rm ox}}$ is the electrostatic gate capacitance associated with gate dielectrics and $C_{G,q}$ is the

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quantum capacitance of the nanotube. For the coplanar geometry, $C_{G,\mathrm{ox}}$ is obtained by

$$C_{G,\mathrm{ox}} = \frac{2\pi\epsilon_0 \cdot \kappa_{\mathrm{avg}} \cdot L}{\ln\left(2 + \frac{4d}{D}\right)} \tag{1}$$

where d is the gate oxide thickness and κ_{avg} is the averaged dielectric constant of the oxide above and below the nanotube. The quantum capacitance is generally a function of gate voltage and drain bias [8], [9]. For our simple arguments, we use $C_{G,q}/L \simeq 4 \times 10^{-16}$ F/μm [10], [11] in the following discussions. With the 10-nm SiO_2 gate oxide, the total capacitance per unit length of our CNFET is given by $C_G/L \sim 0.38 \times 10^{-16}$ F/μm, yielding a gate delay per unit length of $\tau/L = 19$ ps/μm.

Table I lists key performance parameters for our back-gated CNFET device and for two Pd-contacted CNFETs published recently: (A) a CNFET with 8-nm HfO_2 gate oxide by Javey *et al.* [12]; and (B) a CNFET with 18-nm channel length on 12-nm SiO_2 by Seidel *et al.* [13] The gate capacitances C_G/L of devices (A) and (B) listed in Table I are calculated according to (1), taking into account the quantum capacitance. Although Table I provides the first estimation of the ultimate CNFET delay time from static response measurements, more efforts are still needed to obtain the CNFET delay directly from dynamic measurements. Compared with device (B), both our CNFET and the device (A) exhibit higher ON-state currents because of the larger nanotube diameter [6]. Although device (A) possesses a higher g_m value owing to a more effective gate control using thin high-κ dielectrics, our CNFET in fact leads to a smaller gate delay per unit length. Since in an ideal ballistic CNFET, g_m is proportional to C_G, the gate delay is, in principle, independent of the gate capacitance. Therefore, the difference of τ/L between our CNFET and the device (B) may be due to the nanotube quality variation (e.g., defect density) using different synthesis methods or may arise from a higher trap charge density in HfO_2.

TABLE I
COMPARISON OF KEY PERFORMANCE PARAMETERS FOR OUR CNFET, A CNFET WITH 8-nm HfO_2 GATE OXIDE ([DEVICE (A)], AND A 18-nm-GATE CNFET [DEVICE (B)]

	This work	device (A) Ref. [12]	device (B) Ref. [13]
CNT source	Arc discharge	CVD	CVD
CNT diameter (nm)	~ 1.8	~ 1.7	~ 1.1
gate oxide	10-nm SiO_2	8-nm HfO_2	12-nm SiO_2
L (nm)	600	50	18
κ (above/below CNT)	1 / 3.9	15 / 3.9	1 / 3.9
maximum g_{m} (μS)	12.5	27	3.5
C_{G}/L (10^{-16}F/μm)	0.38	1.2	0.32
τ/L (ps/μm)	19	28	59

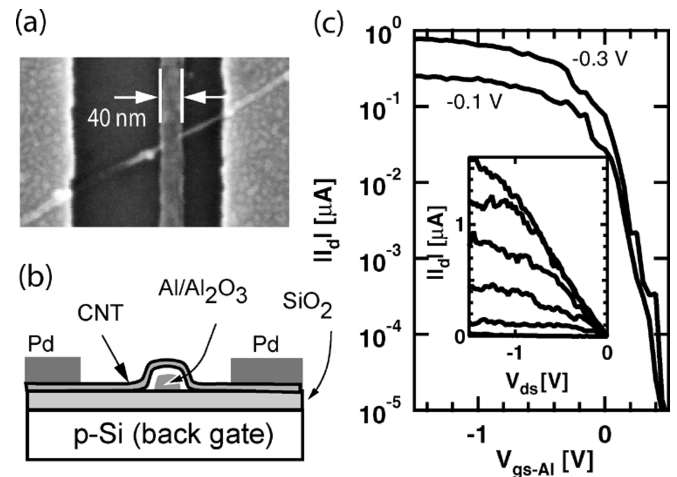

Fig. 2. (a) SEM image of a dual-gate CNFET with a 40-nm-wide Al/Al_2O_3 gate stack. The thicknesses of Al_2O_3 and SiO_2 layers are 4 and 10 nm, respectively. (b) Schematic diagram of the cross section of the dual-gate CNFET. (c) Subthreshold characteristics of the dual-gate CNFET for $V_{\mathrm{ds}} = -0.1$ and -0.3 V. The Si back gate is kept at $V_{\mathrm{gs-Si}} = -2.5$ V. Inset: output characteristics of the dual-gate CNFET for Al gate voltages $V_{\mathrm{gs-Al}} = -1.5$ V to 0 V with a 0.3 V step. The Si back gate is kept at $V_{\mathrm{gs-Si}} = -3.5$ V.

III. DUAL-GATE CNFET

While the gate delay time τ decreases with decreasing gate length L, it is also important to keep the parasitic capacitances small and to avoid any short-channel effects. Most CNFETs studied so far, including the devices listed in Table I, have adopted a fully-gated structure where the gate electrode covers the entire channel region between the source/drain electrodes. We note that for fully gated CNFETs, there is significant (overlap) parasitic capacitance between gate and source electrodes that does not decrease with decreasing L. Therefore, the fully-gated structure as shown in the inset of Fig. 1(a) is not ideal for aggressively scaled CNFET in high-speed applications.

In order to minimize the parasitic capacitances, we utilize a dual-gate structure that enables a much smaller (underlap) capacitance between gate and source electrodes, and fabricate a CNFET with a gate length as short as 40 nm and a source/drain separation of 300 nm. The device image and the schematic structure of the dual-gate CNFET are shown in Fig. 2(a) and (b), respectively, where a 40-nm-wide Al/Al_2O_3 gate stack is placed underneath the nanotube and between the source/drain contacts. Dual-gate CNFETs have been fabricated and studied previously [14], [15], and they possess several advantages over fully-gated CNFETs, such as controllable polarities, a superior subthreshold swing, and improved OFF states [16]. In a dual-gate CNFET, the switching is controlled by the Al gate, and thus, the delay time is determined by the Al gate length L_{g} rather than the source/drain separation L_{ds}. Since L_{g} can be varied independent of L_{ds}, a dual-gate CNFET affords aggressive gate length scaling while allowing at the same time to reduce the parasitic capacitance contributions.

Fig. 2(c) shows I_d versus Al gate voltage $V_{\mathrm{gs-Al}}$ of the 40-nm dual-gate CNFET, exhibiting a subthreshold swing $S = 80$–120 mV/dec. The Si back gate is kept at $V_{\mathrm{gs-Si}} = -2.5$ V

to electrostatically dope the nanotube segments at contact regions as p-type, thereby enabling hole carrier injection. The same doping effects can also be achieved by using chemical dopants [16], [17] instead of the Si back gate in order to further reduce the parasitic capacitance due to the conducting substrate. The inset of Fig. 2(b) shows the output characteristics of the dual-gate CNFET at $V_{\mathrm{gs-Si}} = -3.5$ V, exhibiting current saturation at high drain voltages. The smaller on-currents of the dual-gate CNFET than those shown in Fig. 1(a) may be due to the additional scattering resulting from the tube bending at the edge of the Al gate. Although CNFETs with an even shorter gate length ($\simeq$18 nm) have been fabricated using a fully gated structure [13] [see device (B) in Table I], these devices do not exhibit current saturation in the output characteristics, indicating their operation in the short-channel regime. In comparison, our 40-nm-gate dual-gate CNFETs exhibits excellent transistor characteristics without short-channel effects. This is, to our knowledge, the shortest gate length that has been reported for a well-tempered CNFET (one that does not show short-channel effects) so far.

IV. Conclusion

We have presented a high-performance back-gated CNFET with a peak transconductance of 12.5 μS and the smallest gate delay per unit length ($\sim$ 19 ps/μm) reported thus far. To minimize the parasitic capacitances for scaled CNFET, we utilized a dual-gate design and fabricated a CNFET with 40-nm gate length. The dual-gate CNFET possesses excellent subthreshold and output characteristics without short-channel effects, demonstrating the shortest gate length for a well-tempered CNFET so far.

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