

# 100-GHz Transistors from Wafer-Scale Epitaxial Graphene

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Graphene is the thinnest electronic material, merely one atom thick, with very high carrier mobilities, and therefore it should enable transistors operating at very high frequencies (1–3). Here, we present field-effect transistors (FETs) fabricated on a 2-inch graphene wafer (Fig. 1A) with a cutoff frequency in the radio frequency range, as high as 100 GHz.

Graphene (one to two layers) was epitaxially formed on the Si face of a semi-insulating, high-purity SiC wafer by thermal annealing at 1450°C (4) and exhibited an electron carrier density of  $\sim 3 \times 10^{12} \text{ cm}^{-2}$  and a Hall-effect mobility between 1000 to 1500  $\text{cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ . In order to form the top gate stack, an interfacial polymer layer made of a derivative of poly-hydroxystyrene was spin-coated on the graphene before atomic layer deposition of a 10-nm-thick  $\text{HfO}_2$  insulating layer (5). These gate dielectric deposition steps main-

tained the Hall-effect carrier mobility, between 900 to 1520  $\text{cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ , for devices fabricated across the 2-inch wafer.

Arrays of top-gated FETs were fabricated with various gate lengths,  $L_G$ , the shortest being 240 nm. The drain current,  $I_D$ , of graphene FETs measured as a function of gate voltage,  $V_G$  (Fig. 1B), exhibited  $n$ -type characteristics. For all of our graphene FETs, the Dirac point (the current minimum) always occurred at  $V_G < -3.5 \text{ V}$ . This value corresponds to a rather high electron density ( $> 4 \times 10^{12} \text{ cm}^{-2}$ ) in the graphene channel at a zero gate bias state and is advantageous for achieving low series resistance of graphene FETs. As a result, the device transconductance,  $g_m$ , defined by  $dI_D/dV_G$ , is nearly constant over a wide  $V_G$  range in the on state (right axis in Fig. 1B). The output characteristics (Fig. 1C) differ from those of conventional Si FETs be-

cause of the absence of a band gap in graphene. No clear current saturation was observed at drain biases up to 2 V or before device breakdown, so the device transconductance increases with drain voltage for these graphene FETs.

The scattering ( $S$ ) parameters of these transistors were measured to investigate their high-frequency response. The short-circuit current gain  $|h_{21}|$  (the ratio of small-signal drain and gate currents) was derived from measured  $S$  parameters and displays the  $1/f$  frequency dependence expected for an ideal FET (Fig. 1D). The cutoff frequency  $f_T$  is the frequency at which the current gain  $|h_{21}|$  becomes unity and signifies the highest frequency at which signals are propagated. For a gate length of 240 nm,  $f_T$  as high as 100 GHz was measured at a drain bias of 2.5 V.

This 100-GHz cutoff frequency exceeds those of graphene FETs previously reported (1–3, 5) as well as those of Si metal-oxide semiconductor FETs of the same gate length ( $\sim 40 \text{ GHz}$  at 240 nm) (6). In addition to the current gain, the graphene FETs also possess power gain,  $G_{\text{MAG}}$ , up to  $f_{\text{MAX}} \sim 14 \text{ GHz}$  and 10 GHz for 550-nm and 240-nm gate lengths (7), respectively. Both  $f_T$  and  $f_{\text{MAX}}$  are important figures of merit of transistor performance.  $f_T$  reflects the intrinsic behavior of a transistor channel, whereas  $f_{\text{MAX}}$  also strongly depends on other factors such as the device layout and can be further enhanced, for example, by optimizing the gate contact leads.

The graphene FETs, made by using wafer-scale graphene synthesis and fabrication processes, demonstrate the high potential of graphene for electronics applications.

## References and Notes

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4. Materials and methods are available as supporting material on Science Online.
5. D. B. Farmer *et al.*, *Nano Lett.* **9**, 4474 (2009).
6. [www.itrs.net/Links/2008ITRS/Home2008.htm](http://www.itrs.net/Links/2008ITRS/Home2008.htm)
7.  $f_{\text{MAX}}$  does not exhibit a particular scaling behavior with the gate length, in contrast to that of  $f_T$ . Also see (4).
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## Supporting Online Material

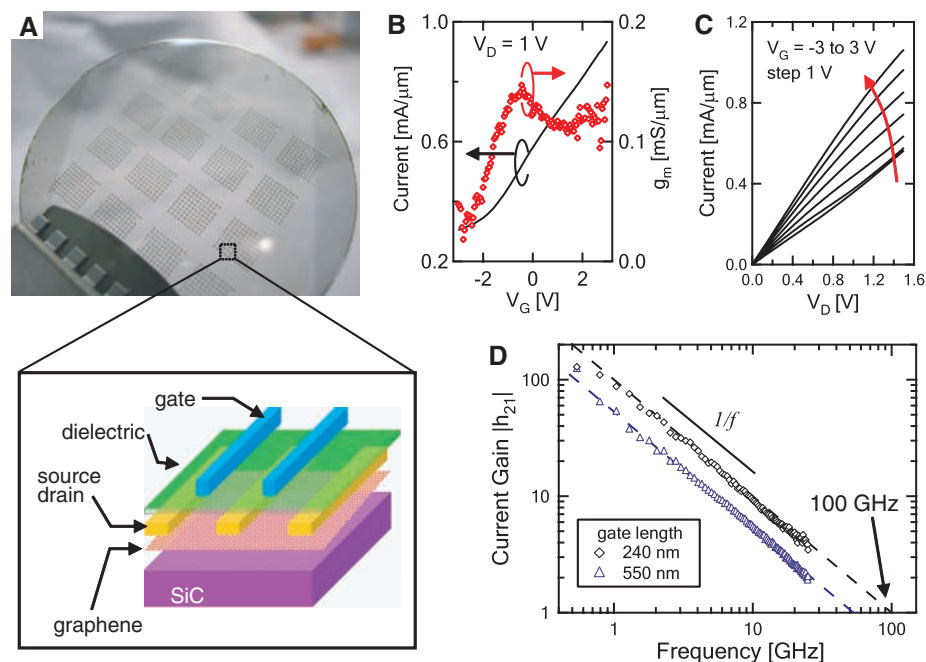
[www.sciencemag.org/cgi/content/full/327/5966/662/DC1](http://www.sciencemag.org/cgi/content/full/327/5966/662/DC1)  
Materials and Methods

SOM Text  
Figs. S1 to S6  
References

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**Fig. 1.** (A) Image of devices fabricated on a 2-inch graphene wafer and schematic cross-sectional view of a top-gated graphene FET. (B) The drain current,  $I_D$ , of a graphene FET (gate length  $L_G = 240 \text{ nm}$ ) as a function of gate voltage at drain bias of 1 V with the source electrode grounded. The device transconductance,  $g_m$ , is shown on the right axis. (C) The drain current as a function of  $V_D$  of a graphene FET ( $L_G = 240 \text{ nm}$ ) for various gate voltages. (D) Measured small-signal current gain  $|h_{21}|$  as a function of frequency  $f$  for a 240-nm-gate ( $\diamond$ ) and a 550-nm-gate ( $\triangle$ ) graphene FET at  $V_D = 2.5 \text{ V}$ . Cutoff frequencies,  $f_T$ , were 53 and 100 GHz for the 550-nm and 240-nm devices, respectively.