Dual-Gate Graphene FETs With f_T of 50 GHz

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***Abstract*—A dual-gate graphene field-effect transistor is presented, which shows improved radio-frequency (RF) performance by reducing the access resistance using electrostatic doping. With a carrier mobility of 2700 $cm^2/V \cdot s$, a cutoff frequency of 50 GHz is demonstrated in a 350-nm-gate-length device. This f_T value is the highest frequency reported to date for any graphene transistor, and it also exceeds that of Si MOS field-effect transistors at the same gate length, illustrating the potential of graphene for RF applications.**

***Index Terms*—Access resistance, dual gate, field-effect transistor (FET), graphene, radio frequency (RF).**

I. Introduction

GRAPHENE is a monolayer of carbon atoms in a honeycomb lattice, which has attracted considerable attention over the last few years due to its unique electronic properties [1]. With a high saturation velocity (5.5×10^7 cm/s) [2], graphene is considered a very promising candidate for millimeter-wave applications. In addition, the ultrathin body thickness of graphene offers ideal 2-D electrostatics for the ultimately scaled down device. Recently, cutoff frequencies in the gigahertz regime have been demonstrated in top-gated graphene transistors built on exfoliated single-layer graphene sheets [3], [4] and few-layer graphene grown on SiC substrates [5]. It was found that, in top-gated graphene field-effect transistors (FETs), the radio-frequency (RF) performance was primarily limited by the mobility degradation of graphene after oxide deposition [3], [6]. Recently, Kim *et al.* [7] have reported progress in enhancing the carrier mobility in top-gated graphene FETs (GFETs) by using a thin layer of naturally oxidized Al_2O_3 as the nucleation layer for the deposition of high-k gate dielectrics. Another important factor that strongly affects the overall RF performance of graphene transistors is the access resistance between the source/drain contacts and the gated graphene channel. The access regions are required to minimize the capacitance between the gate and source/drain electrodes in a top-gated FET structure. However, because this access region consists of only a monolayer of ungated graphene, the sheet resistance is much higher than that of heavily doped Si used in conventional MOSFETs and is comparable to the resistance of the gated graphene channel. Access resistance becomes particularly important when the gate length shrinks, and it may hinder further improvement of RF performance with the downscaling of gate length in graphene transistors.

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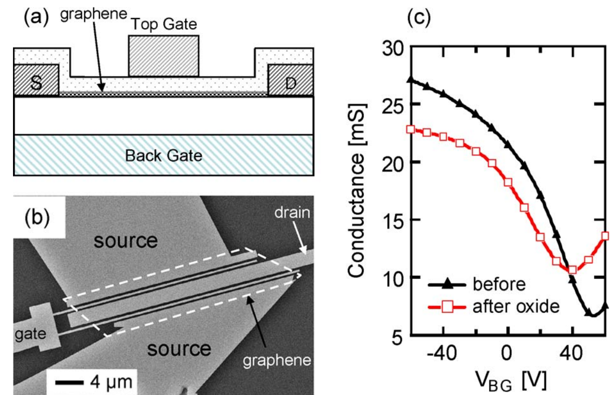

Fig. 1. (a) Device schematic of the dual-gate graphene transistor. (b) SEM image of a double-channel graphene transistor. The channel width is 27 μm, and the gate length is 350 nm for each channel. (c) Measured channel conductance as a function of the back-gate voltage of a graphene device before and after the deposition of 12-nm-thick ALD Al_2O_3. Prior to the ALD process, a layer of 2-nm Al is deposited and oxidized as the nucleation layer.

This letter describes the use of a dual-gate GFET to investigate the impact of access resistance on RF performance. In this structure, the access resistance of the graphene transistor is modulated by the back gate through electrostatic doping. By varying the back-gate voltage, the access resistance is reduced by more than half, leading to a fourfold increase of transconductance in a 350-nm-gate GFET. Combined with a carrier mobility of 2700 $cm^2/V \cdot s$ enabled by an improved oxide deposition process, a cutoff frequency of 50 GHz in the dual-gate GFET is achieved.

II. Device Fabrication

The device structure of the dual-gate GFET is shown in Fig. 1(a). Single-layer graphene was deposited by mechanical exfoliation on high-resistivity Si substrates ($> 10\ k\Omega \cdot cm$) covered with 300-nm-thick thermal oxide. The source and drain electrodes made of Pd/Au metals (20 nm/40 nm thick) were fabricated by e-beam lithography and liftoff. The oxide deposition process described in [7] was adopted here to form a layer of 12-nm-thick Al_2O_3 by atomic layer deposition (ALD) as the top-gate dielectric. Fig. 1(c) shows that the device transfer characteristics were not appreciably degraded after this dielectric process. Finally, the Pd/Au (20-nm/40-nm) metal stack was deposited as the top-gate electrode. Fig. 1(b) shows the SEM image of the double-channel graphene transistor with a gate length of $L_g = 350$ nm. The width of each channel is 27 μm, and the spacing between the top-gate electrode and the source/drain contacts is 300 nm.

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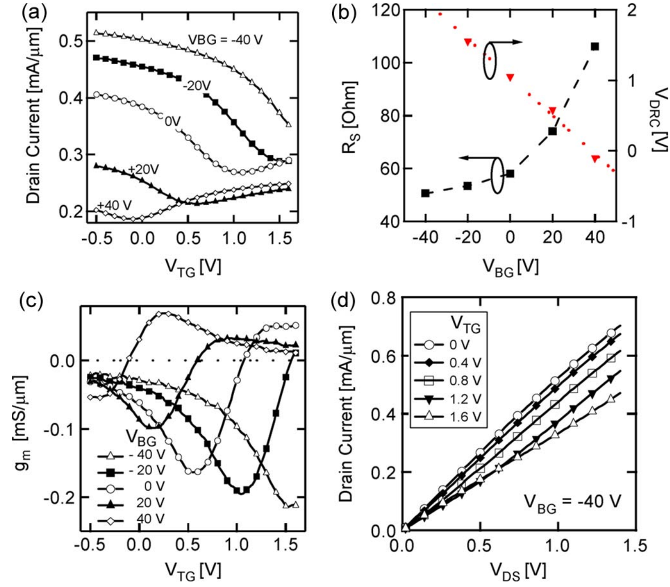

Fig. 2. (a) Transfer characteristics of the GFET at various back-gate voltages and $V_D = 0.8$ V. (b) Series resistance of the GFET and Dirac voltage $V_{\rm DRC}$ as a function of back-gate voltage. (c) Transconductance of the GFET at various back-gate voltages. The drain bias is 0.8 V. (d) Output characteristics at $V_{\rm BG} = -40$ V.

III. Results and Discussion

A Si substrate is used as the global back gate, while the top gate serves as the main gate terminal for regular FET operations. Fig. 2(a) shows the transfer characteristics of the GFET at different back-gate voltages $V_{\rm BG}$. At $V_{\rm BG} = 0$ V, the GFET exhibits ambipolar transfer characteristics with a current minimum at $V_{\rm TG} = 0.7$ V. This ambipolar transport reflects the gapless nature of the graphene band structure. The current minimum corresponds to the Dirac point, where the total carrier density of electrons and holes in the graphene channel becomes minimal. Dirac voltage $V_{\rm DRC}$, defined as the top-gate voltage at the Dirac point, is linearly dependent on $V_{\rm BG}$, as shown in Fig. 2(b), and the slope $(\Delta V_{\rm BG}/\Delta V_{\rm DRC} \cong 35)$ can be used to determine the capacitance $C_{\rm TG}$ of the top-gate dielectrics. Using the back-gate capacitance value of $C_{\rm BG} = 11.6$ nF/cm^2, $C_{\rm TG}$ is estimated to be 0.40 μF/cm^2.

In Fig. 2(a), the current at the Dirac point decreases with increasing $V_{\rm BG}$, indicating an increasing series resistance with $V_{\rm BG}$. This is because the back gate not only shifts the threshold voltage of the graphene transistor but also modulates the graphene that is not covered by the top gate. This additional resistance is analogous to the access resistance in conventional Si MOSFETs. The total resistance of the graphene device (R_T) is modeled as the sum of an ideal graphene channel resistance modulated by the top gate and a series resistance R_S [2], [7], and R_T is given by

$$R_T = R_S + \left[e\mu \frac{W}{L_G} \sqrt{n_0^2 + \left[\frac{C_{\rm tot}}{e} \cdot (V_{\rm TG} - V_{\rm DRC}) \right]^2} \right]^{-1} \quad (1)$$

where μ is the field-effect mobility and n_0 is the minimum sheet carrier density determined by disorder and thermal excitation. $C_{\rm tot}$ is the total top-gate capacitance given by $C_{\rm tot}^{-1} = C_{\rm TG}^{-1} + C_Q^{-1}$, where C_Q is the quantum capacitance of graphene. For a relevant carrier density of $\sim 5 \times 10^{12}$ cm^{-2}, $C_Q \cong 3$ μF/cm^2. Based on (1), a minimum carrier density $n_0 \sim 5 \times 10^{11}$ cm^{-2} and a field-effect mobility $\mu \sim 2700$ cm^2/V $\cdot$ s, both independent of $V_{\rm BG}$, was obtained for the graphene channel using the extraction method described in [2] and [7]. In the following, we show that, while the mobility remains constant as $V_{\rm BG}$ varies, the device performance can be improved by optimizing other device parameters. Fig. 2(b) shows the extracted series resistance R_S of the graphene device as a function of $V_{\rm BG}$, where R_S increases with increasing $V_{\rm BG}$ up to 40 V. This $V_{\rm BG}$ gate dependence of R_S due to ungated graphene is consistent with the trend shown in Fig. 1(c). It is noted that R_S also includes the contact resistance between graphene and metal electrodes. To achieve the optimal RF performance in dual-gate graphene transistors, it is necessary to bias $V_{\rm BG}$ properly so that R_S is at its minimum.

Fig. 2(c) shows the transconductance g_m of the graphene device at different back-gate voltages. The impact of series resistance on device performance is evident, as can be seen in the increasing peak values of the p-branch g_m when $V_{\rm BG}$ decreases from 40 to -40 V. At $V_{\rm BG} = -40$ V and $V_{\rm TG} = 1.5$ V, the GFET reaches a peak g_m of -0.22 mS/μm. It is noted that, while the series resistance is reduced by roughly half from $V_{\rm BG} = 40$ to -40 V, the peak p-type g_m is enhanced by four times, changing from -0.05 to -0.22 mS/μm. The output characteristics at $V_{\rm BG} = -40$ V are shown in Fig. 2(d).

To assess the RF characteristics of the GFET, on-chip microwave measurements were carried out up to 30 GHz. The measured S-parameters were de-embedded using specific "short" and "open" structures with identical layouts, excluding the graphene channel, to remove the effects of parasitic capacitance and resistance associated with the pads and connections. The use of high-resistivity Si substrates allows for a dc back-gate bias while, at the same time, enabling RF operation without significant signal loss. Based on the results in Fig. 2(c), $V_{\rm BG}$ was kept at -40 V in order to achieve the highest RF performance in the dual-gate GFET. Fig. 3(a) shows the current gain $|h_{21}|$ from the measured S-parameters at $V_{\rm TG} = 1.6$ V and a drain bias $V_{\rm DS} = 0.8$ V, yielding a cutoff frequency f_T of 50 GHz. The de-embedded current gain $|h_{21}|$ exhibits the -20-dB/dec frequency dependence, as expected for a well-behaved FET. This f_T value is the highest frequency reported to date for any graphene transistor, and it also exceeds that of Si MOSFETs ($\sim$25 GHz) at the same gate length of 350 nm [8]. Fig. 3(b) shows the peak g_m of p-type GFETs as a function of the series resistance modulated by $V_{\rm BG}$. The well-known relation $f_T = g_m/(2\pi C)$ established for conventional FETs has recently been demonstrated to be also valid for graphene devices [3]. Based on the measured f_T of 50 GHz for $g_m = 0.22$ mS, the right axis of Fig. 3(b) shows the projected f_T as a function of R_S, illustrating a fourfold improvement in f_T as R_S decreases from 110 to 50 Ω.

IV. Conclusion

A dual-gate graphene transistor has been fabricated, showing improved RF performance by optimizing the series resistance.

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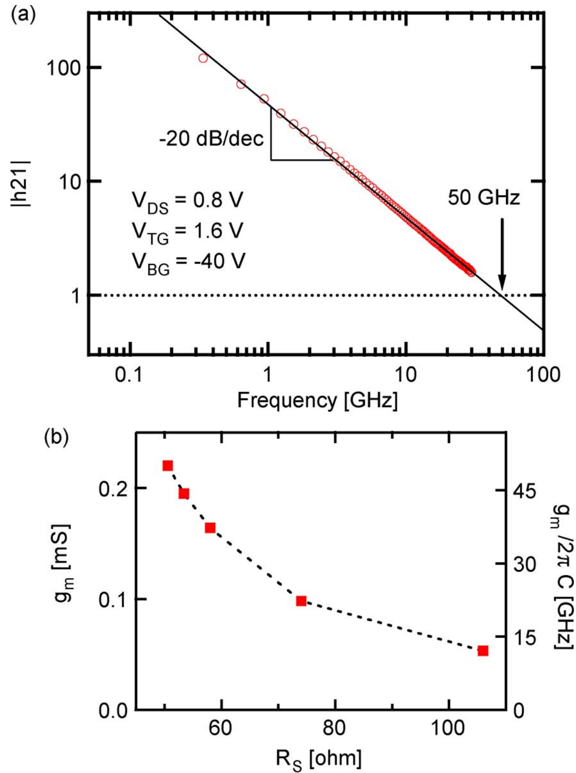

Fig. 3. (a) RF performance of a 350-nm-gate GFET, showing a current gain at −20 dB/dec and a cutoff frequency f_T of 50 GHz. (b) Peak transconductance as a function of series resistance R_S derived from Fig. 2(b) and (c). The projected cutoff frequency $f_T = g_m/2\pi C$ is shown on the right axis.

A cutoff frequency of 50 GHz has been demonstrated for a gate length of 350 nm. This value exceeds that of Si MOSFETs at the same gate length, illustrating the potential of graphene for RF applications. In addition, while a global back gate has been used here to optimize the access resistance in a dual-get GFET, the results can be generalized to other GFET structures. It is expected that similar performance enhancement can be achieved through other techniques, such as local bottom gates or selective doping [9], to modulate the resistance in the access regions.

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REFERENCES

[1] A. H. Castro Neto, F. Guinea, N. M. R. Peres, K. S. Novoselov, and A. K. Geim, "The electronic properties of graphene," *Phys. Mod. Phys.*, vol. 81, no. 1, pp. 109–163, Jan. 2009.

[2] I. Meric, M. Han, A. F. Young, B. Ozyilmaz, P. Kim, and K. L. Shepard, "Current saturation in zero-bandgap, top-gated graphene field-effect transistors," *Nature Nanotechnol.*, vol. 3, no. 11, pp. 654–659, Nov. 2008.

[3] Y.-M. Lin, K. A. Jenkins, A. Valdes-Garcia, J. P. Small, D. B. Farmer, and P. Avouris, "Operation of graphene transistors at gigahertz frequencies," *Nano Lett.*, vol. 9, no. 1, pp. 422–426, Jan. 2009.

[4] I. Meric, N. Baklitskaya, P. Kim, and K. L. Shepard, "RF performance of top-gated, zero-bandgap graphene field-effect transistors," in *IEDM Tech. Dig.*, 2008, pp. 1–4.

[5] J. S. Moon, D. Curtis, M. Hu, D. Wong, C. McGuire, P. M. Campbell, G. Jernigan, J. L. Tedesco, B. VanMil, R. Myers-Ward, C. Eddy, Jr., and D. K. Gaskill, "Epitaxial-graphene RF field-effect transistors on Si-face 6H-SiC substrates," *IEEE Electron Device Lett.*, vol. 30, no. 6, pp. 650–652, Jun. 2008.

[6] M. C. Lemme, T. J. Echtermeyer, M. Baus, and H. Kurz, "A graphene field-effect device," *IEEE Electron Device Lett.*, vol. 28, no. 4, pp. 282–284, Apr. 2007.

[7] S. Kim, J. Nah, I. Jo, D. Shahrjerdi, L. Colombo, Z. Yao, E. Tutuc, and S. K. Banerjee, "Realization of a high mobility dual-gated graphene field-effect transistor with Al_2O_3 dielectric," *Appl. Phys. Lett.*, vol. 94, no. 6, p. 062 107, Feb. 2009.

[8] [Online]. Available:http://www.itrs.net/Links/2008ITRS/Home2008.htm

[9] D. B. Farmer, R. Golizadeh-Mojarad, V. Perebeinos, Y.-M. Lin, G. S. Tulevski, J. C. Tsang, and P. Avouris, "Chemical doping and electron–hole conduction asymmetry in graphene devices," *Nano Lett.*, vol. 9, no. 1, pp. 388–392, Jan. 2009.

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