Development of Graphene FETs for High Frequency Electronics

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Abstract

Recent advances in fabricating, measuring, and modeling of top-gated graphene FETs for high-frequency electronics are reviewed. By improving the oxide deposition process and reducing series resistance, an intrinsic cut-off frequency as high as 50 GHz is achieved in a 350-nm-gate graphene FET at a drain bias of 0.8 V. This f_T value is the highest frequency reported to date for any graphene transistor, and it also exceeds that of Si MOSFETs at the same gate length, illustrating the potential of graphene for RF applications.

Introduction

Graphene is a two-dimensional (2D) material, consisting of a sheet of carbon atoms arranged in a honeycomb lattice, and possesses exciting potential for electronics. Fig. 1 shows the band structure of single-layer graphene. Unlike conventional semiconductors, graphene is a zero-gap semiconductor with a linear energy-momentum dispersion relation given by $E = v_F \cdot \hbar k$, where $v_F \sim 10^6$ m/s is the Fermi velocity. The carriers in graphene behave as relativistic particles, leading to exotic transport phenomenon, such as anomalous quantum Hall effects[1,2]. While there have been enormous research activities on graphene originated from the keen curiosity towards these unusual physical properties, graphene is also considered a very promising candidate for high-frequency devices due to its exceptional electrical properties, such as a high intrinsic carrier mobility (> 10,000 cm^2/Vs at room temperature)[3] and a large saturation velocity (~ 5.5×10^7 cm/s)[4]. Furthermore, the ultra-thin body thickness of graphene offers ideal two-dimensional electrostatics for the ultimately scaled-down device.

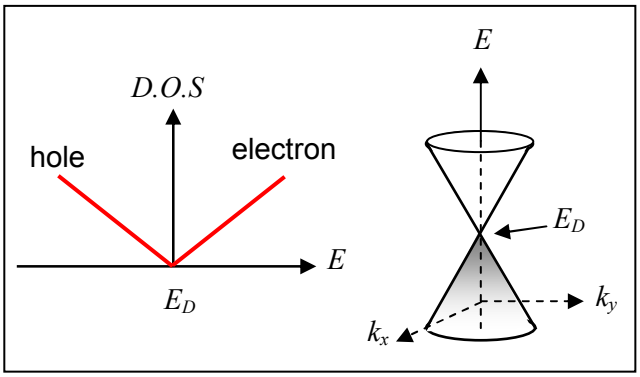

Fig. 1: Density of state and band structure of a single-layer graphene.

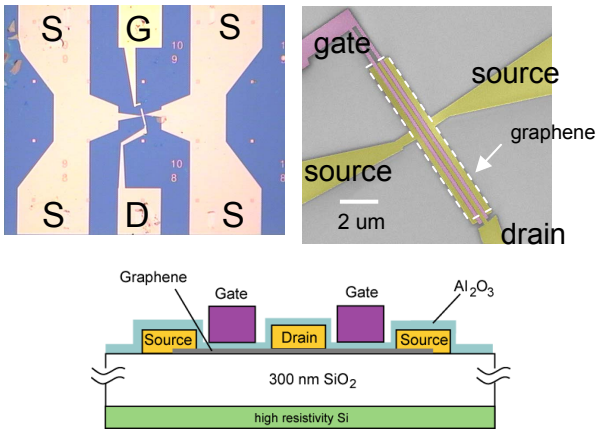

Fig. 2: Optical and SEM image of a top-gated graphene transistor. The bottom figure shows the schematic cross-section of the device.

While single-layer graphene was first successfully isolated and identified by micromechanical exfoliation of bulk graphite[1,2], different synthesis approaches have also been developed and realized, such as sublimation of Si of SiC substrates[5] and CVD on metal films[6,7], to produce large-area or even wafer-scale graphene layers. The rapid advances in graphene synthesis, together with its outstanding electrical properties, have opened up practical opportunities for circuits and applications based on graphene, and made it one of the most exciting materials in emerging technologies.

Recently, graphene FETs with cut-off frequencies in the GHz regime have been reported by several groups[8-10]. Here we review the progress in fabricating, measuring, and modeling of graphene FETs for high-frequency electronics, and report graphene devices with a cut-off frequency (f_T) up to 50 GHz.

Fabrication of Top-gated Graphene FET

Fig. 2 shows the SEM image and the device structure of top-gated graphene transistors with a layout pertinent to high-frequency measurements, where single layer graphene was prepared by mechanical exfoliation. Graphene devices fabricated from epitaxially-grown graphene layers on SiC substrates [9] and CVD-grown

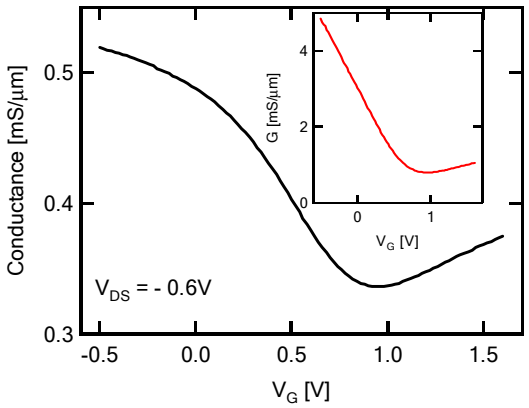

Fig. 3: Conductance of a graphene transistor measured as a function of top gate voltage. The gate length L_g is 350 nm and the source/drain distance is 1μm. The inset shows the linear gate voltage dependence of channel conductance after subtracting the series access resistance.

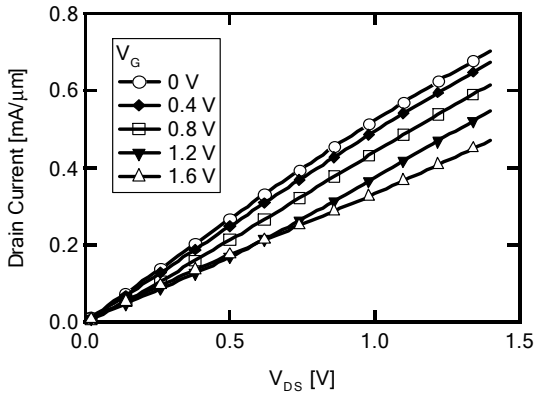

Fig. 4: Output characteristics of the same graphene transistor as shown in Fig. 3.

graphene films on metals have also been demonstrated [6,7] to exhibit similar transport properties. The source and drain electrodes made of Pd/Au metals (20nm/40nm thick) were fabricated by e-beam lithography and lift-off. A layer of 12-nm Al_2O_3, formed by ALD (atomic layer deposition), is deposited as the top-gate dielectric. Finally, the Pd/Au (20 nm/40 nm) metal stack was deposited as the top-gate electrode. The typical transfer and output characteristics of graphene FETs are shown in Figs. 3 and 4. The transfer characteristics exhibit the "V" shape behavior, reflecting the ambipolar transport in graphene. As shown in the inset of Fig. 3, after subtracting series resistance that consists of contact resistance and the resistance of the un-gated graphene segments, the channel conductance is linearly dependent on gate voltage.

RF Measurements and Modeling

The high-frequency response of the graphene transistor is evaluated by on-chip scattering parameter measurements in the GHz range. Short and open device

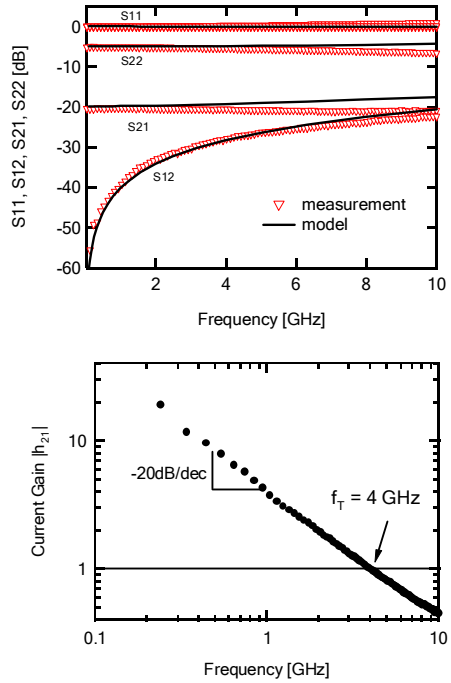

Fig. 5: Measured scattering parameters, S11, S12, S21 and S22, of a graphene transistor. The bottom figure shows the measured current gain |h21| as a function of frequency, featuring a cut-off frequency of 4 GHz.

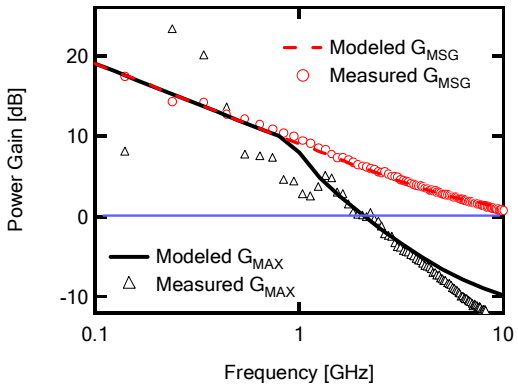

Fig. 6: Comparison of measured and modeled power gains of the graphene transistor as a function of frequency.

structures are used to de-embed the intrinsic device behavior from the extrinsic parasitic capacitance and resistance. Figs. 5 and 6 show the magnitude of the four S-parameters and the corresponding current gain $|h_{21}|$, respectively, of a 350-nm-gate graphene FET as a function of frequency, featuring a cut-off frequency f_T of 4 GHz. The current gain of the device exhibits the ideal frequency dependence of -20dB/decade of a well-behaved FET. To gain insights into the behavior of the top-gated graphene FETs, a small-signal circuit model was developed [11], and the S-parameters are simulated and plotted as solid lines in Fig. 5, showing good agreement with the measured data up to the cut-off frequency. Fig. 6 shows the measured device power gain, according to different

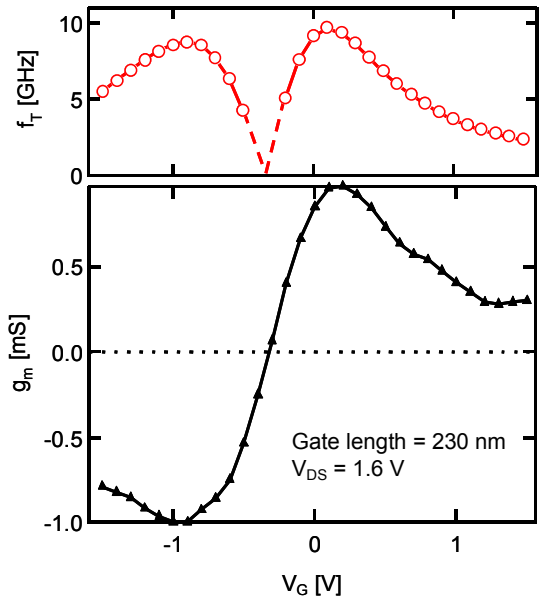

Fig. 7: The gate dependence of cut-off frequency and the extrinsic transconductance of a graphene transistor.

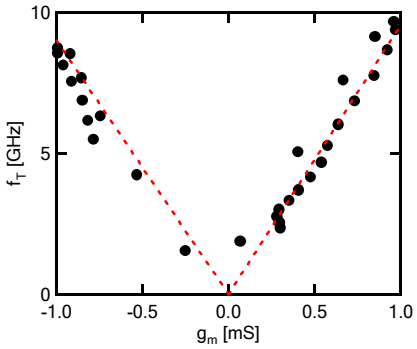

Fig. 8: The correlation of the cut-off frequency and the device transconductance.

definitions [12], compared with modeled results. Good correlation is also obtained for Maximum Stable Gain (G_{MSG}) and Maximum Available Gain (G_{MAX}), with the estimated f_{MAX} at 2 GHz. The agreement between the modeled and measured data not only is encouraging, but it also provides key device parameters for developing more complicated circuits based on graphene.

Fig. 7 shows measured f_T and the transconductance g_m of a 230-nm-gate graphene FET as a function of gate voltage at V_{DS} = 1.6 V. The negative and positive branches of the transconductance represent the p- and n-type carrier transport of the graphene FET, respectively. As the gate voltage varies, the measured f_T displays a trend following the absolute value of g_m, with the two peaks in f_T around 10 GHz corresponding to the valley and the peak of the g_m curve. Fig. 8 shows the correlation between g_m and f_T, exhibiting a symmetric, linear dependence for both n- and p-branches. This linear dependence provides the

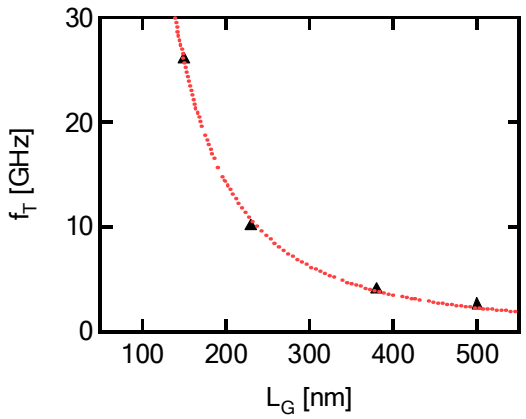

Fig. 9: Gate length dependence of cut-off frequency of graphene transistors fabricated using the same processing conditions.

evidence that the high-frequency response of graphene FETs can be related to that of conventional MOSFETs, and the cut-off frequency is given by the relation $f_T = g_m/(2\pi C)$. In particular, this dependence also suggests that, similar to conventional FETs, in order to enhance RF performance, it is necessary to improve the g_m/C ratio, which can be attained in graphene devices by reducing gate length or improving the channel mobility, as explained below.

In principle, the maximum cut-off frequency of an FET can be improved by reducing the gate length. Fig. 9 shows the measured peak f_T as a function of gate length for graphene devices fabricated under identical processing conditions, where the peak f_T increases from ~3 GHz to 26 GHz as the gate length shrinks from 500 nm to 150 nm. The peak f_T is inversely proportional to the square of the gate length L_G, and this $f_T \sim 1/L_G^2$ dependence arises from the fact that these graphene transistors are operating in the triode regime (see Fig. 4) [8].

Towards High-Performance Graphene FETs

In top-gated graphene FETs, the device performance is primarily limited by the mobility degradation of graphene during the device fabrication process, particularly after oxide deposition, and a significant series resistance compared to channel resistance. For example, Fig. 10 compares the transfer characteristics of two graphene FETs before and after the oxide deposition with two different deposition processes, A and B. In the process A, the graphene surface is first functionalized with NO_2 to promote the uniform oxide coverage in the subsequent ALD process of Al_2O_3. In process B, a layer of 2-nm naturally-oxidized Al_2O_3 is used prior to ALD[13]. It is found that process B better maintains the intrinsic transport properties of graphene by improving the interface between graphene and the oxide.

Another important factor that strongly affects the overall RF performance of graphene FETs is the access

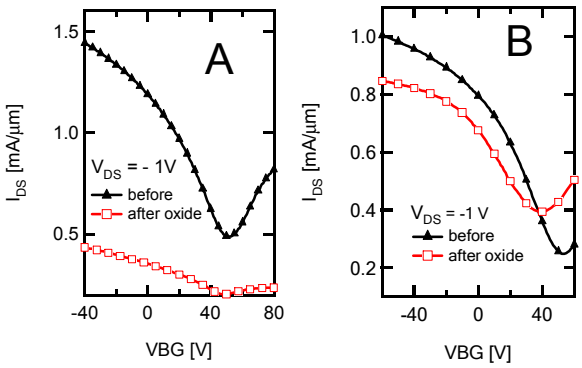

Fig. 10: The impact of top gate dielectrics on the transport properties of graphene using two different oxide deposition processes, A and B.

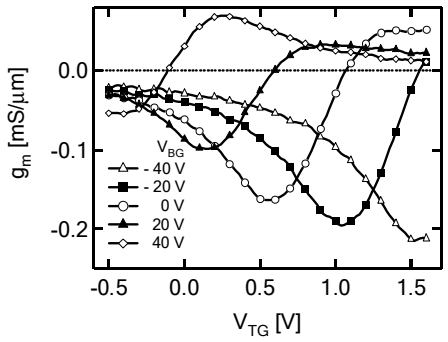

Fig. 11: Measured transconductance of a 350-gate-length graphene FET at various back-gate voltages. The drain bias is 0.8V.

resistance between the source/drain contacts and the gated graphene channel. Since this access region consists of only a monolayer of un-gated graphene, the sheet resistance is much higher than that of heavily doped Si used in conventional MOSFETs, and is comparable to the resistance of gated graphene channel. This issue of access resistance becomes particularly critical when the gate length shrinks, and may hinder further improvement of RF performance with the down-scaling of gate length. For graphene FETs fabricated on SiO_2/Si substrates, the series resistance associated with ungated segments can be reduced by electrostatic doping using the Si substrate as the back gate. Fig. 11 shows the transconductance g_m of the graphene device at different back-gate voltages V_{BG}. The impact of the series resistance on the device performance is evident, as can be seen in the increasing peak values of the p-branch g_m when V_{BG} decreases from 40 V to -40V. At V_{BG} = -40V and V_{TG} = 1.5, the graphene FET reaches a peak g_m of -0.22 mS/μm.

With the oxide deposited using process B and a minimal series resistance at V_{BG} = -40V, Fig. 12 shows the current gain $|h_{21}|$ of a 350-nm-gate graphene FET from the measured S-parameters at V_{TG} = 1.6 V and a drain bias V_{DS} = 0.8 V, yielding a cut-off frequency of 50 GHz. This f_T is

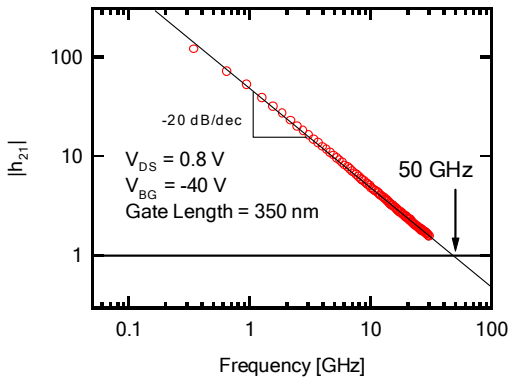

Fig. 12: A high-performance graphene transistor showing a cut-off frequency of 50 GHz. The gate length is 350 nm.

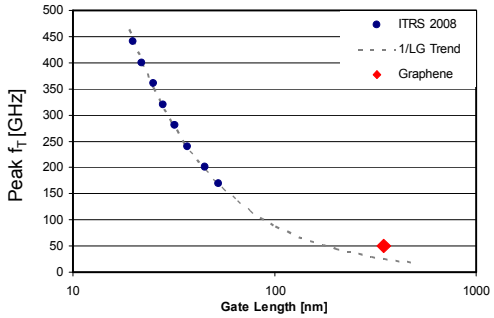

Fig. 13: Comparison of the performance of graphene transistors and Si MOSFETs.

not only the highest value reported for any graphene FETs to date, but it also exceeds that of Si MOSFETs (~25 GHz) at the same gate length according to the 2008 International Roadmap for Semiconductors (ITRS) [14](see Fig. 13), illustrating the potential of graphene for RF applications.

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