Enhanced Performance in Epitaxial Graphene FETs With Optimized Channel Morphology

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***Abstract*—This letter reports the impact of surface morphology on the carrier transport and radio-frequency performance of graphene FETs formed on epitaxial graphene synthesized on SiC substrates. Such graphene exhibits long terrace structures with widths between 3–5 μm and steps of 10 $\pm$ 2 nm in height. While a carrier mobility value above 3000 $\mathrm{cm^2/V \cdot s}$ at a carrier density of 10^{12} $\mathrm{cm^{-2}}$ is obtained in a single graphene terrace, the step edges can result in a step resistance of $\sim$21 k$\Omega \cdot \mu$m. By orienting the transistor layout so that the entire channel lies within a single graphene terrace and by reducing the access resistance associated with the ungated part of the channel, a cutoff frequency above 200 GHz is achieved for graphene FETs with channel lengths of 210 nm, i.e., the highest value reported on epitaxial graphene thus far.**

***Index Terms*—Field-effect transistor (FET), graphene, radio-frequency (RF).**

GRAPHENE has received significant attention as a promising candidate for future high-speed electronics [1]–[3]. Since the first demonstration of graphene transistors for RF applications [4], [5], the performance has been rapidly improved, with cutoff frequencies greater than 100 GHz reported by several groups [6]–[8]. The successful development of graphene-based electronics relies on the availability of large-area and high-quality materials. Two types of graphene, i.e., epitaxial [9]–[11] and chemical vapor deposited (CVD) [12], have been proposed for wafer-scale production. In spite of the exceptional electrical properties of graphene, the device performance is strongly affected by both the morphology of the film and its interaction with the environment (e.g., substrate and dielectric interfaces). The performance of CVD graphene devices is particularly sensitive to the transfer process, which can result in the presence of wrinkles, lattice defects, and chemical impurities. Epitaxial graphene grown on the surface of SiC substrates typically yields larger domain sizes and does not require transfer to another substrate. However, the morphology of as-prepared epitaxial graphene usually contains steps [11] and other morphological features such as domain boundaries, which may have a negative impact on device performance.

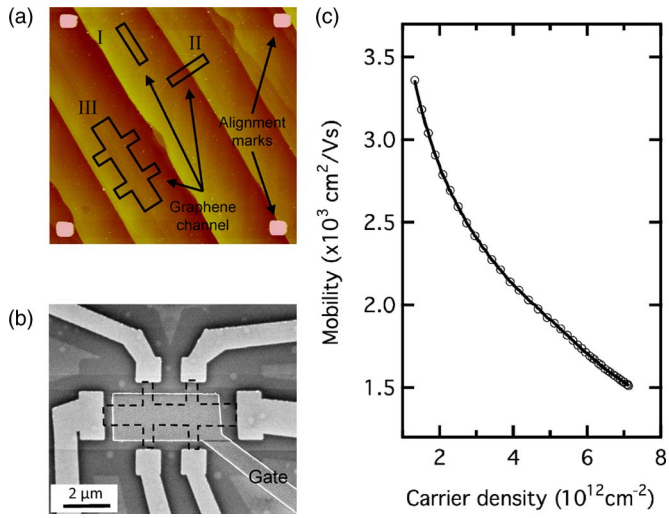

Fig. 1. (a) AFM image of epitaxial graphene grown on SiC, showing the terrace structure and steps. The scanning area is 21 μm $\times$ 21 μm. The solid lines sketch the outline of graphene channels of different devices. Channels I and III both lie within a single terrace, whereas the channel II contains one step along the transport direction. (b) SEM image of a gated Hall bar fabricated on a single terrace. The graphene channel is highlighted by the dashed line. (c) Carrier mobility measured as a function of carrier density for the device shown in (b).

The impact of this morphology on carrier transport in epitaxial graphene is studied here, and it is found that a single-terrace step with a height of $\sim$10 nm can lead to a resistance on the average of 21 k$\Omega \cdot \mu$m. To avoid performance degradation due to such steps, a transistor layout is designed so that the entire device channel lies within a single terrace or domain. Combined with a reduction of access resistances associated with ungated channel regions, cutoff frequencies above 200 GHz are achieved, demonstrating improved RF performance compared with graphene field-effect transistors (FETs) without such channel morphology and gate structure optimization.

Epitaxial graphene is synthesized on 2-in semi-insulating 6H-SiC (II–VI, Inc.) wafers. Prior to the graphene growth, the wafer is etched in hydrogen at 1620 °C to remove $\sim$200 nm of SiC. Graphene is then grown on the Si-face of the substrate at 1620 °C in a flowing Ar ambient at 50 mbar, yielding films consisting of one to two layers of graphene [13]. The morphology of the as-prepared graphene/SiC surface is characterized

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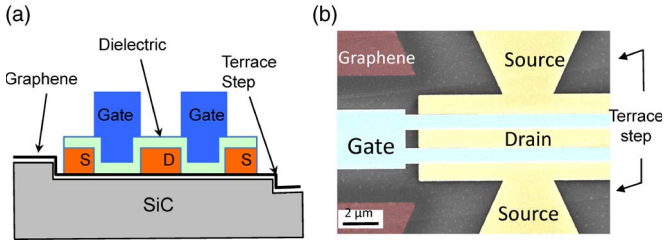

Fig. 2. (a) Schematic cross-section of a top-gated GFET. To reduce the access resistance associated with the ungated regions, the gate electrodes overlap with the source and the drain by ∼50 nm. (b) (false color) SEM image of a dual-channel graphene FET where both channels are located within a single terrace. The channel length is 750 nm, and the total channel width is 30 μm.

by atomic force microscopy (AFM) [see Fig. 1(a)], revealing wide and smooth terraces that extend long distances ($> 50\ \mu$m) parallel to the step edges. The width of these terraces range between 3 and 5 μm, and the step height is 10 nm $\pm$ 2 nm.

Two types of two-terminal graphene devices with orthogonal channel orientations are fabricated, as illustrated by the regions outlined and labeled as I and II in Fig. 1(a). The channels of resistor I are parallel to the step edge and located within a single terrace, whereas those of resistor II contain one step edge along the transport direction. In both types of devices, the channel dimensions are all 500 nm in width and 2 μm in length. Resistance measurements are performed at room temperature in vacuum for more than ten devices, yielding distinct resistance values for both device types. Device I possesses an average resistance of 5 kΩ, significantly lower than the average resistance of 48 kΩ for device II. This clearly shows that carrier transport is severely affected by scattering associated with terrace steps within the channel, which leads to an additional channel resistance on the average of 21 k$\Omega \cdot \mu$m for a single step.

To eliminate the nonideal factors associated with the steps, top-gated Hall bar devices are fabricated on a single-terrace domain, as depicted by the channel outline III in Fig. 1(a). Fig. 1(b) shows a scanning electron microscopy (SEM) image of such a device, where the entire channel lies within a single terrace. The gate dielectric used here consists of a 10-nm-thick interfacial polymer layer and 10 nm of HfO_2 grown by atomic layer deposition (ALD) [14]. At $V_g = 0$ V, the graphene film is n-type with a carrier concentration of 5.6×10^{12} cm^{-2}. Fig. 1(c) shows the measured carrier mobility μ_e as a function of carrier density n, where μ_e increases from 1500 to 3300 cm^2/V $\cdot$ s as n decreases from 7.1×10^{12} to 1.3×10^{12} cm^{-2} by changing V_g.

To evaluate the RF performance of step-free graphene films, graphene FETs (GFETs) are fabricated using the methods described in [6]. Fig. 2(a) shows a schematic of the device cross section. To achieve optimal performance, the graphene channels are placed within single terraces. To eliminate access resistance due to the ungated channel regions, the gate electrode is designed to overlap with the source/drain electrodes by ∼50 nm. Fig. 2(b) shows a SEM image of a dual-channel GFET, where both channels lie within a single terrace.

Figs. 3(a) and (b) show the output characteristics of GFETs with the channel lengths L_C of 750 and 210 nm, respectively. The gate voltage is swept between -4 and 4 V with a step of 1 V. The current density increases with decreasing L_C, as expected. For $L_C = 210$ nm, the current density is more

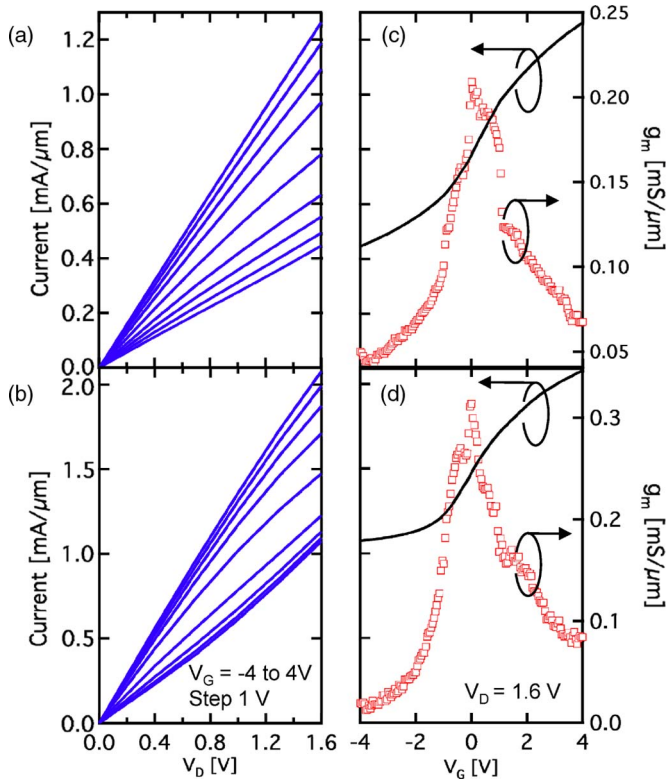

Fig. 3. (a) and (b) Measured output characteristics of GFETs with different channel lengths: (a) 750 and (b) 210 nm. (c) and (d) Measured transfer characteristics of these graphene FETs at $V_d = 1.6$ V. The transconductance is shown on the right axes as a function of gate voltage.

than 2 mA/μm at $V_d = 1.6$ V and $V_g = 4$ V [see Fig. 3(b)]. The current modulation ratio, which is defined by $I_d(V_g = 4\ \text{V})/I_d(V_g = -4\ \text{V})$, is ∼3 for $L_C = 750$ nm and decreases to ∼2 for $L_C = 210$ nm. The reduction of the current modulation as L_C decreases is due to the contact resistance between graphene and metal electrodes, which becomes more dominant as L_C decreases. In Fig. 3(b), the total contact resistance $2R_C$ is estimated to be ∼700 $\Omega \cdot \mu$m. Figs. 3(c) and (d) show the transfer characteristics at $V_d = 1.6$ V for $L_C = 750$ and 210 nm, respectively. The corresponding transconductances g_m of these devices are plotted on the right axes in Figs. 3(c) and (d). These transconductances exhibit maximum values at $V_g \sim 0$ V of 210 and 320 μS/μm for $L_C = 750$ and 210 nm, respectively. In comparison, the device reported in [6], which was fabricated on epitaxial graphene without morphology or structure optimization, possessed a lower current density of ∼1 mA/μm and a maximum g_m value of ∼200 μS/μm at $V_d = 1.6$ V for $L_C = 240$ nm.

The RF performance of the GFETs is characterized by on-chip S-parameter measurements up to 30 GHz, following the standard deembedding procedures described in [6]. Fig. 4 plots the measured current gain $|h_{21}|$ as a function of frequency for GFETs with different L_C at $V_d = 2.5$ V and $V_g = 0$ V after deembedding. The current gain follows the expected $1/f$ frequency dependence, and the cutoff frequency f_T is determined by the extrapolation of $|h_{21}|$, yielding f_T of 60 and 210 GHz for $L_C = 750$ and 210 nm, respectively. Because of the deembedding, this cutoff frequency represents the response of the intrinsic device under the gate electrode. The f_T of

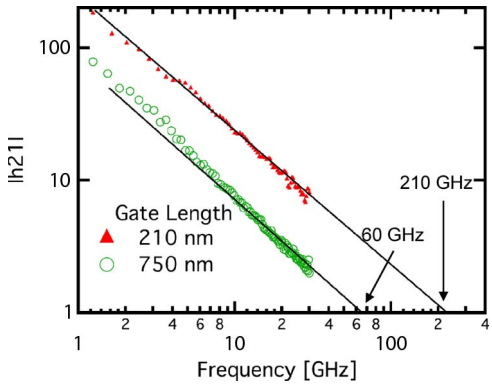

Fig. 4. Measured current gain $|h_{21}|$ of GFETs at $V_d = 2.5$ V, showing the $1/f$ frequency dependence.

210 GHz is the highest value reported for epitaxial GFETs thus far. Previously, $f_T = 100$ GHz was achieved for GFETs with $L_C = 240$ nm using a similar gate dielectric [6]. This illustrates the performance enhancement afforded by the optimization of channel morphology and device structure presented in this letter. The frequency-length product of these GFETs are $\sim$45 (GHz $\cdot$ μm), which is comparable to the highest value of 43 obtained from exfoliated graphene [7] and much higher than those of Si ($\sim$8.9) and InP ($\sim$17) [15].

Steps and other topographical features such as domain boundaries and surface wrinkles will influence graphene transport not only on SiC epitaxial graphene but also in CVD grown and transferred graphene. It is therefore imperative that the effect of these features is understood and that the morphology of the graphene layer is controlled.

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REFERENCES

[1] K. Bolotin, K. Sikes, Z. Jiang, M. Klima, G. Fudenberg, J. Hone, P. Kim, and H. Stormer, "Ultrahigh electron mobility in suspended graphene," *Solid State Commun.*, vol. 146, no. 9/10, pp. 351–355, Jun. 2008.

[2] A. K. Geim and K. S. Novoselov, "The rise of graphene," *Nat. Mater.*, vol. 6, no. 3, pp. 183–191, Mar. 2007.

[3] P. Avouris, "Graphene: Electronic and photonic properties and devices," *Nano Lett.*, vol. 10, no. 11, pp. 4285–4294, Sep. 2010.

[4] Y.-M. Lin, K. A. Jenkins, A. Valdes-Garcia, J. P. Small, D. B. Farmer, and P. Avouris, "Operation of graphene transistors at gigahertz frequencies," *Nano Lett.*, vol. 9, no. 1, pp. 422–426, Jan. 2009.

[5] I. Meric, N. Baklitskaya, P. Kim, and K. L. Shepard, "RF performance of top-gated, zero-bandgap graphene field-effect transistors," in *IEDM Tech. Dig.*, 2008, pp. 1–4.

[6] Y.-M. Lin, C. Dimitrakopoulos, K. A. Jenkins, D. B. Farmer, H.-Y. Chiu, A. Grill, and P. Avouris, "100-GHz transistors from wafer-scale epitaxial graphene," *Science*, vol. 327, no. 5966, p. 662, Feb. 2010.

[7] L. Liao, Y.-C. Lin, M. Bao, R. Cheng, J. Bai, Y. Liu, Y. Qu, K. L. Wang, Y. Huang, and X. Duan, "High-speed graphene transistors with a self-aligned nanowire gate," *Nature*, vol. 467, no. 7313, pp. 305–308, Sep. 2010.

[8] Y. Wu, Y.-M. Lin, A. A. Bol, K. A. Jenkins, F. Xia, D. B. Farmer, Y. Zhu, and P. Avouris, "High-frequency, scaled graphene transistors on diamond-like carbon," *Nature*, vol. 472, no. 7341, pp. 74–78, Apr. 2011.

[9] C. Berger, Z. Song, X. Li, X. Wu, N. Brown, C. Naud, D. Mayou, T. Li, J. Hass, A. N. Marchenkov, E. H. Conrad, P. N. First, and W. A. de Heer, "Electronic confinement and coherence in patterned epitaxial graphene," *Science*, vol. 312, no. 5777, pp. 1191–1196, May 2006.

[10] C. Dimitrakopoulos, Y.-M. Lin, A. Grill, D. B. Farmer, M. Freitag, Y. Sun, S.-J. Han, Z. Chen, K. A. Jenkins, Y. Zhu, Z. Liu, T. J. McArdle, J. A. Ott, R. Wisnieff, and P. Avouris, "Wafer-scale epitaxial graphene growth on the Si-face of hexagonal SiC (0001) for high frequency transistors," *J. Vac. Sci. Technol. B*, vol. 28, no. 5, pp. 985–992, Sep. 2010.

[11] K. V. Emtsev, A. Bostwick, K. Horn, J. Jobst, G. L. Kellogg, L. Ley, J. L. McChesney, T. Ohta, S. A. Reshanov, J. Röhrl, E. Rotenberg, A. K. Schmid, D. Waldmann, H. B. Weber, and T. Seyller, "Towards wafer-size graphene layers by atmospheric pressure graphitization of silicon carbide," *Nat. Mater.*, vol. 8, no. 3, pp. 203–207, Mar. 2009.

[12] X. Li, W. Cai, J. An, S. Kim, J. Nah, D. Yang, R. Piner, A. Velamakanni, I. Jung, E. Tutuc, S. K. Banerjee, L. Colombo, and R. S. Ruoff, "Large-area synthesis of high-quality and uniform graphene films on copper foils," *Science*, vol. 324, no. 5932, pp. 1312–1314, Jun. 2009.

[13] D. K. Gaskill, G. Jernigan, P. Campbell, J. L. Tedesco, J. Culbertson, B. VanMil, R. L. Myers-Ward, C. Eddy, Jr., J. Moon, D. Curtis, M. Hu, D. Wong, C. McGuire, J. Robinson, M. Fanton, T. Stitt, D. Snyder, X. Wang, and E. Frantz, "Epitaxial graphene growth on SiC wafers," *ECS Trans.*, vol. 19, no. 5, pp. 117–124, 2009.

[14] D. B. Farmer, H.-Y. Chiu, Y.-M. Lin, K. A. Jenkins, F. Xia, and P. Avouris, "Utilization of a buffered dielectric to achieve high field-effect carrier mobility in graphene transistors," *Nano Lett.*, vol. 9, no. 12, pp. 4474–4478, Dec. 2009.

[15] *ITRS Roadmap*. [Online]. Available: http://www.itrs.net/Links/2008ITRS/Home2008.htm